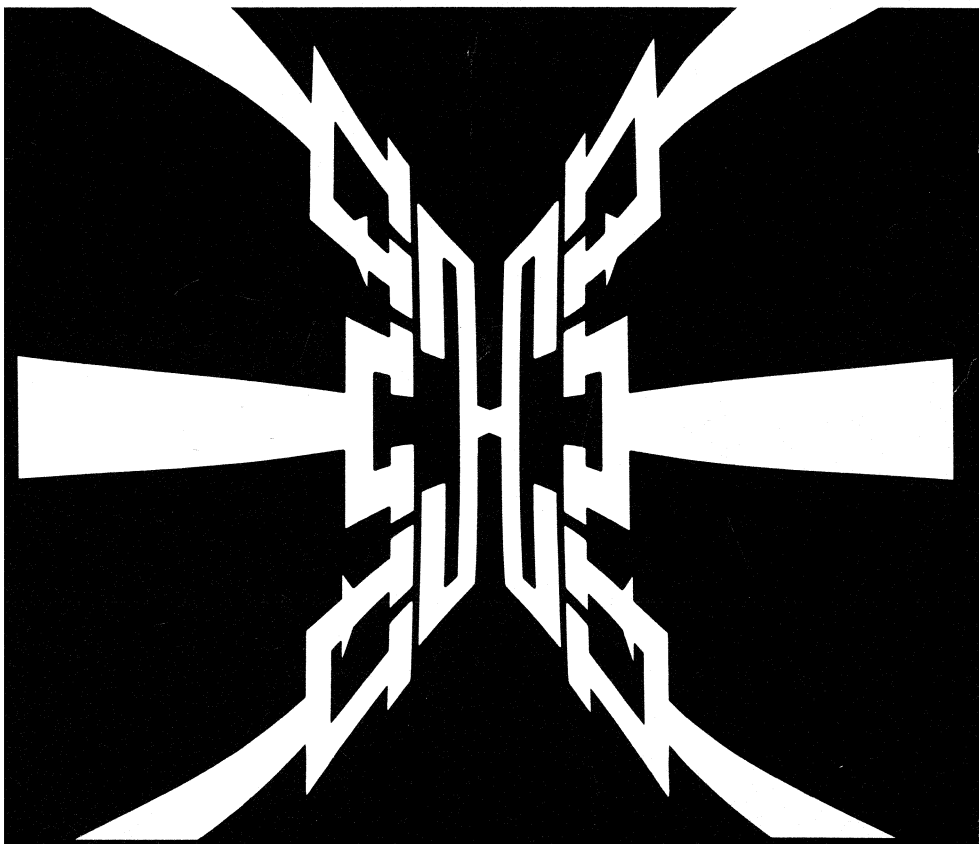
RCA

COS/MOS Integrated Circuits Manual



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RCA

COS/MOS Integrated Circuits Manual

This Manual, like its preceding edition, has been prepared to provide an understanding of the basic principles involved in the design, fabrication, and application of COS/MOS digital integrated circuits. The basic fundamentals, features and characteristics, building-block elements, and logic-system design rules for complementary-symmetry/metal-oxide-semiconductor (COS/MOS) integrated circuits are explained. Design examples and performance data are then given for the use of COS/MOS integrated circuits in a variety of circuit applications, including NOR and NAND gates, arithmetic units, multivibrators, sinusoidal oscillators, counters and registers, digital display systems, and frequency synthesizers. The Manual also features a **Circuits** section that provides design ideas for the use of COS/MOS integrated circuits in twenty-five practical circuit applications.

This new edition has been updated and substantially expanded to include descriptive data on recently announced RCA COS/MOS integrated circuits and to provide broader more extensive applications information. This Manual is intended primarily as a guide to circuit and system designers; it is also useful to students, educators, technicians, and others interested in the use of solid-state devices and circuits.

RCA | Solid State Division | Somerville, NJ 08876

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Fundamentals of COS/MOS Integrated Circuits

The evolution of solid-state circuits using discrete bipolar transistors was marked by major advances when both n-p-n and p-n-p devices became available and circuit designers were able to exploit the numerous advantages to be gained by connecting them together in "complementary-symmetry" arrangements. In monolithic IC's using bipolar transistors, it has not been possible to exploit the numerous advantages of complementary-symmetry circuits because conflicting technological factors currently mitigate against the fabrication of optimized n-p-n and p-n-p bipolar transistors on the same substrate. However, the complementary-symmetry circuit advantages can be harnessed in IC's by integrating compatible p-channel and n-channel enhancement-type MOS field-effect transistors on a monolithic substrate. After considerable pioneering research and developmental efforts, in 1968 RCA announced commercial availability of COS/MOS (Complementary-Symmetry/Metal-Oxide-Semiconductor) IC's, monolithic integrated circuits containing p- and n-channel MOS transistors.

COS/MOS circuits, in configurations which encompass both logic and memory, are excellently suited to use in digital circuit applications and are characterized by their micropower quiescent operation, moderately fast propagation delay, excellent noise immunity, large fanout capability, and operation from a single power supply over a wide voltage range. The characteristics of COS/MOS logic and memory circuits are comparatively immune to variations in temperature. Both standard and custom COS/MOS circuits of medium-scale integration (MSI) and large-scale integration (LSI) complexity operate with simple single-phase clocking.

BASIC PRINCIPLES OF MOS FIELD-EFFECT TRANSISTORS

Field-effect transistors combine the inherent advantages of solid-state devices (small size, low power consumption, and mechanical rug-

gedness) with a very high input impedance. Unlike bipolar devices in which performance depends on the interaction of two types of charge carriers, holes and electrons, field-effect transistors are unipolar devices; i.e., operation is basically a function of only one type of charge carrier, holes in p-channel devices and electrons in n-channel devices.

Basic Structure

Early models of field-effect transistors used a reverse-biased semiconductor junction for the control electrode. In **MOS** (metal-oxide-semiconductor) field-effect transistors, a metal control "**gate**" is separated from the semiconductor "**channel**" by an insulating **oxide** layer, as shown in Fig. 1. One of the major features of the metal-oxide-semiconductor structure is that the very high

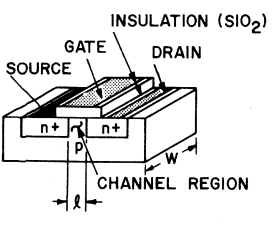


Fig. 1 – Structure of an MOS field-effect transistor.

input resistance of MOS transistors (unlike that of junction-gate-type field-effect transistors) is not affected by the polarity of the bias on the control (gate) electrode. In addition, the leakage currents associated with the insulated control electrode are relatively unaffected by changes in ambient temperature. Because of their unique properties, MOS field-effect transistors are particularly well suited for use in digital switching applications, as well as in linear voltage amplifiers and voltage-controlled attenuators.

Functional Description

The operation of field-effect devices can be explained in terms of a charge-control concept. The metal control electrode, which is called a gate, acts as a charge-storage or control element. A charge placed on the gate induces an equal but opposite charge in the semiconductor layer, or channel, located beneath the gate. The charge induced in the channel can then be used to control the conduction between two ohmic contacts, called the source and the drain, made to opposite ends of the channel.

The MOS type of field-effect transistor uses a metal gate electrode separated from the semiconductor material by an insulator, as shown in Fig. 1. Like the p-n junction, this insulated-gate electrode can deplete the source-to-drain channel of active carriers when suitable bias voltages are applied. However, the insulated-gate electrode can also increase the conductivity of the channel without increasing steady-state input current or reducing power gain.

The two basic types of MOS field-effect transistors are the **depletion** type and the **enhancement** type. All COS/MOS integrated circuits are of the enhancement type. In this type, the gate must be forward-biased to produce active carriers and permit conduction through the channel. No useful channel conductivity exists at either zero or reverse gate bias.

Because MOS transistors can be made to utilize either electron conduction **(n-channel)** or hole conduction **(p-channel)**, two distinct enhancement-type MOS field-effect transistors are possible. As shown in Fig. 2, the schematic symbol for an MOS transistor indicates whether it has an n-channel or a p-channel. The direction of the arrowhead in the

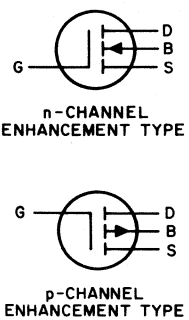


Fig. 2 — Schematic symbols for MOS transistors (G : gate, D : drain, B : active bulk or substrate, S : source).

symbol identifies the n-channel device (arrow pointing toward the channel) or the p-channel device (arrow pointing away from the channel).

Fig. 3 shows a cross-sectional view of an n-channel enhancement-type MOS transistor (reversal of n-type and p-type regions would produce a p-channel enhancement-type transistor). This type of transistor is normally non-conducting until a sufficient voltage of the correct polarity is applied to the gate electrode. When a positive bias voltage is applied to the gate of an n-channel enhancement transistor, electrons are drawn into the channel region beneath the gate. If sufficient

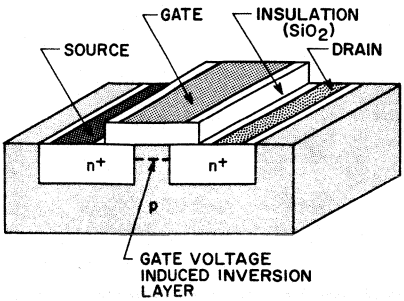


Fig. 3 — Cross-sectional view of an n-channel enhancement-type MOS transistor.

voltage is applied, this channel region changes from p-type to n-type and provides a conduction path between the n-type source and the n-type drain regions. (In a p-channel enhancement transistor, the application of negative bias voltage draws holes into the region below the gate so that this channel region changes from n-type to p-type and again provides a source-to-drain conduction path.) The broken line connecting the drain and source in the schematic symbol for the MOS transistor (Fig. 2) is representative of the fact that the channel is open until conduction is "enhanced" by application of the appropriate bias. Effectively, the increase in gate voltage causes the forward transfer characteristic to shift along the gate-voltage axis in the manner shown in Fig. 4. Because of this feature, enhancement-type MOS transistors are particularly suitable for switching applications.

In enhancement-type transistors, the gate electrode must cover the entire region between the source and the drain so that the applied gate voltage can induce a conductive channel between them.

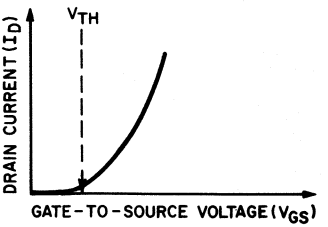


Fig. 4 – Drain current as a function of gate-to-source voltage in an MOS transistor.

If all the conductivity types in an MOS transistor are reversed, the resulting device is "**complementary**" in characteristics to the original device. Thus, n-channel MOS devices are related to p-channel MOS devices in the same way that p-n-p transistors are related to n-p-n transistors.

Circuits like the one shown in Fig. 5 that use both types of MOS devices are called **complementary** circuits. A COS/MOS integrated circuit in its simplest form consists of the configuration shown in Fig. 5;

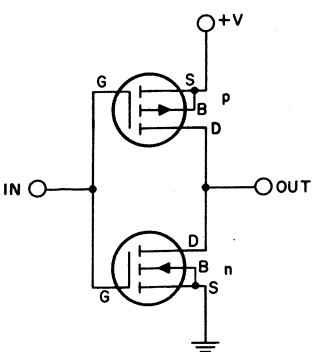


Fig. 5 – Complementary-symmetry inverter circuit using MOS transistors.

the active switching elements consist of two opposite-polarity MOS transistors connected in series with both p- and n-channel gate terminals tied together. If the drain of one transistor and the drain of the other in the COS/MOS IC are connected, the result is a simple complementary **inverter** circuit; this circuit is discussed in detail later.

Design Equations

An MOS device is basically a voltage-controlled device that exhibits a capacitive input and conducts initially when the gate-to-source voltage is equal to the threshold voltage, V_{TH}. This threshold voltage point is shown graphically in Fig. 4.

Current-Voltage Relationships – Fig. 6 shows the theoretical curve of **drain-to-source current** I_D as a function of **drain-to-source voltage** V_{DS} and **gate-to-source voltage** V_{GS}

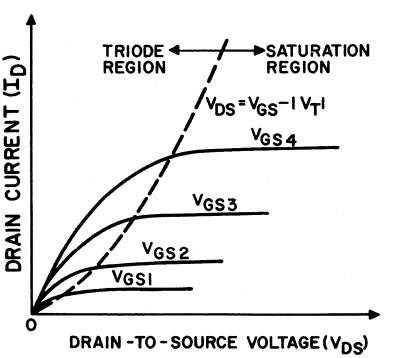


Fig. 6 – Drain-to-source current as a function of drain-to-source voltage in a p-channel enhancement-type MOS transistor.

for a p-channel enhancement-type MOS transistor. The "ideal" equations for these characteristics in the various operating regions are as follows:

1. In the **triode region**, i.e., $0 \leq V_{DS} \leq (V_{GS} - |V_{TH}|)$, the

drain-to-source current is defined by the following relationship:

$$I_D = K\frac{W}{L}\left[2(V_{GS} - |V_{TH}|)V_{DS} - V_{DS}^2\right] \quad (1)$$

2. In the **saturation region**, i.e., $0 \leq (V_{GS} - |V_{TH}|) \leq V_{DS}$, the drain-to-source current is given by

$$I_D = K\frac{W}{L}(V_{GS} - V_{TH})^2 \quad (2)$$

3. When the gate-to-source voltage is less than the threshold voltage, i.e., $V_{GS} \leq |V_{TH}|$, the drain-to-source current becomes

$$I_D = 0 \quad (3)$$

In Eqs. (1) and (2),

$$K = \frac{\mu\epsilon}{2t_{ox}} \quad (4)$$

where μ is the effective surface mobility of the carriers in the channel, ϵ is the permittivity of the oxide, t_{ox} is the thickness of the oxide, W is the width of the channel, and L is the length of the channel.

Threshold Voltage – The threshold voltage for a p-channel enhancement-type unit is given by

$$V_{TH} = V_{TO} - K_B\left[(V_{BS} + \psi\ 1/2 - (\psi)1/2\right] \quad (5)$$

where K_B is a function of the carrier concentration of the substrate, V_{BS} is the substrate-to-source voltage, ψ is the surface potential, and V_{TO} is the negative threshold value for $V_{BS} = 0$. The change in V_{TH} as a function of V_{BS} is plotted for several n-type substrate resistivities in Fig. 7. The boundary between the regions in

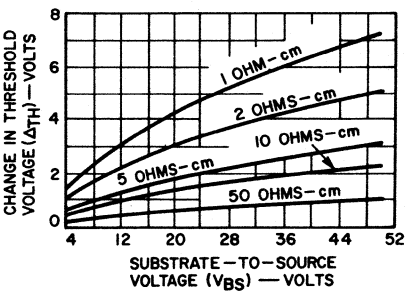


Fig. 7 – Change in V_{TH} with V_{BS} for several n-type substrate resistivities.

which Eqs. (1) and (2) apply corresponds to the condition $V_{DS} = V_{GS} - |V_{TH}|$, and appears as the dashed line in Fig. 6. The equations are ideal in that the finite drain resistance in the saturation region ($0 \leq V_{GS} - |V_{TH}| \leq V_{DS}$), the series parasitic resistance, the variation of channel mobility with gate-to-source voltage, and the drain-to-source leakage current are all neglected.

Threshold voltage can also be defined as follows:

$$V_{TH} = \frac{t_{ox}S}{\epsilon} + \psi_{MS} + 2\psi_f \quad (6)$$

where ψ_{MS} is the difference between metal and semiconductor work functions, ψ_f is the difference in Fermi potential between the inverted

surface and the bulk of the semiconductor, and

$$S = \psi_{SS} + \psi_B \qquad (7)$$

where ψ_{SS} is the fixed surface-state charge, and ψ_B is the bulk charge of silicon.

It can be demonstrated that, by differentiating Eq. (1), the resistance R in the region where $V_{GS} - |V_{TH}| \leq V_{DS}$ is given approximately by

$$R \approx \frac{1}{\frac{\mu\epsilon W}{t_{ox}L}(V_{GS} - |V_{TH}|)} \qquad (8)$$

The **resistance** of an MOS structure is a function of gate-to-source bias and channel geometry; it is independent of drain-to-source potential. Thus, an MOS device can be used as a fixed or variable resistor, with the amount of resistance controlled by the gate-to-source bias.

Input Capacitance – For switching purposes, it is important to know the input capacitance. This value can be represented to the first order by the capacitance of the oxide, C_{ox}, which is given by

$$C_{ox} = \frac{\epsilon WL}{t_{ox}} \qquad (9)$$

This value is increased by the capacitance of the gate metallization which extends beyond the channel, as well as the case and stray wiring capacitances. For present MOS transistors, t_{ox} is in the order of 500 to 2500 angstroms and L is in the order of 0.1 to 1 mil. When L is decreased, the current capability is increased and the input capacitance is decreased; however, the drain-to-source breakdown voltage is decreased.

Figure of Merit – The figure of merit ω_o for an MOS transistor is given as

$$\omega_o = \frac{g_m}{C_{ox}} \qquad (10)$$

where g_m is the transconductance and is given by

$$g_m = \frac{\partial I_{SD}}{\partial V_{GS}} \Bigg|_{V_{DS} = \text{constant}} \qquad (11)$$

or

$$g_m = \frac{\mu\epsilon W}{t_{ox}L}(V_{GS} - |V_{TH}|) \qquad (12)$$

FABRICATION OF COS/MOS INTEGRATED CIRCUITS

All the COS/MOS circuits discussed in this Manual are monolithic integrated circuits. The distinguishing feature of any monolithic integrated circuit is that all components required to perform a particular circuit function are combined and interconnected on a common substrate. The constituent elements of the resultant circuits lose their identities as discrete components, and the over-all circuits, in essence, become microminiaturized function blocks. The monolithic technology, which makes possible simultaneous fabrication of conglomerates of solid-state devices within or on a very small chip of semiconductor material (usually silicon), is essentially an extension of the basic planar technology used in

the fabrication of discrete silicon transistors.

The manufacture of silicon monolithic integrated circuits involves a series of highly critical operations in which silicon is subjected to carefully controlled, high-temperature chemical processes. The lateral physical dimensions of the chemical reactions in the silicon are controlled by photolithographic techniques. High-precision photomasks represent the assembly tools, jigs, and fixtures in the manufacture of monolithic integrated circuits.

General IC Wafer Processing

Monolithic integrated circuits are not fabricated singly, but rather "by the wafer" as a minimum "batch." The fabrication process involves a sequence of diffusion and photolithographic engraving steps. Individual silicon wafers are cut from a silicon ingot into slices. Each wafer is then polished to a mirror finish. Circuit complexity determines the size of the **chip** for a particular design. Circuits being produced today use chip sizes up to about 180 mils square. For this range of chip sizes, the number of chips produced per wafer varies from the order of 1,000 down to about 100. Because the cost of processing a wafer is the same regardless of the number of chips it produces, it is evident that small chip area reduces the cost of the individual chips. In addition, defects tend to be random in nature; as a result, the probability of a defect is larger for a large chip area than for a small one. Thus, a smaller chip area increases processing yields and further reduces costs.

The first major step in processing the mirror-finished wafer involves the formation of a silicon dioxide layer on the surface of the wafer, as shown in Fig. 8. This thin layer of silicon dioxide protects the silicon surface of the finished integrated circuit, acts as a barrier to **dopants** during the

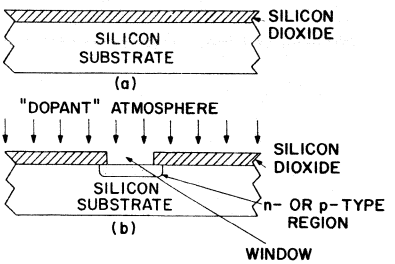


Fig. 8 — (a) Formation of the silicon-dioxide layer on the surface of a wafer; (b) layer used as mask.

semiconductor junction-forming processes, and provides an insulating substrate for the interconnection metals. Silicon dioxide is formed on the silicon wafer by heating it to a temperature of 1000 to 1300°C and passing oxygen over the surface. The silicon dioxide layer also serves as a "pattern mask" in determining the area through which "dopant" atoms may pass freely into the silicon substrate to form regions of either n-type or p-type silicon (depending on the type of dopant material used).

The ability to control the procedures by which "**windows**" are formed selectively in the silicon dioxide layer is one of the most crucial in integrated-circuit manufacturing. In some instances, the windows may be in the order of only 0.1 mil square. The windows in the silicon dioxide define the geometrical areas in which chemical diffusion

reactions are localized. These windows are mechanically positioned and dimensioned by the use of **photomasks** and photochemical procedures, a system of processing which is dependent on the photosensitive properties of a type of lacquer called **photoresist.**

Fig. 9(a) illustrates the manner in which an oxide-coated silicon wafer is covered with a layer of photoresist lacquer several thousand angstroms thick. A photomask, in this case a glass plate having a pattern of black spots on it, is placed against the photoresist, and the system is exposed to ultraviolet light. Illuminated areas of the photoresist tend to harden (polymerize), while the areas under the black spots of the photomask remain soft and are removed during a subsequent "photo-development" operation. Fig. 9(b) shows the "exposed" patterns of the windows in the photoresist following the "photo-development" operation. The wafer is then subjected to a chemical **etchant** (such as diluted hydrofluoric acid), which dissolves the silicon oxide in the photoresist windows without attacking the silicon underneath. The desired windows in the silicon oxide are thus produced, as shown in Fig. 9(c). The remaining photoresist is removed chemically in Fig. 9(d). This "cleaned" wafer with windows in its oxide coating is then ready for chemical doping procedures in diffusion furnaces to produce regions with either n-type or p-type electrical characteristics in the areas beneath the windows.

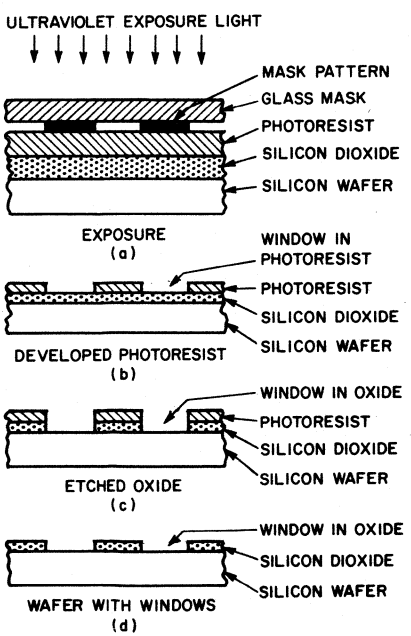


Fig. 9 — Photoresist processing of monolithic integrated-circuit wafer.

Chemical **diffusion** processes are used to introduce the semiconductor junction-forming dopants into the bulk silicon. A series of these diffusion cycles is performed in processing of integrated-circuit wafers.

COS/MOS IC Wafer Processing

The starting material (substrate) for a monolithic COS/MOS integrated circuit consists of a uniform single crystal of n-type silicon; the orientation of the n-type crystal structure is about the (100) axis. Diffusion processing techniques (doping) permit introduction of certain impurities to desired depths and surface concentrations. Vertical penetration of the impurities is controlled by the diffusion temperature and time; control of lateral diffusion is made possible by a combination of the masking properties of silicon dioxide and photochemical techniques. The

silicon-dioxide insulating material on the surface of the substrate is selectivity opened (windows are formed) for each diffusion step. The oxide is subsequently replaced except in metal-contact areas.

The following paragraphs summarize the basic processes involved in the formation and interconnection of electronic components on a basic COS/MOS integrated circuit, such as the one shown in Fig. 10. The fabrication of a simple n-channel and p-channel device pair with gate protection is described.

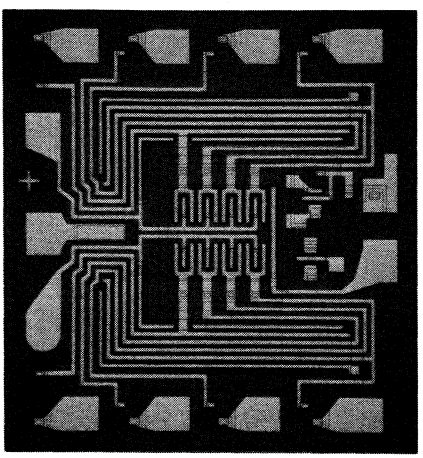


Fig. 10 — Photograph of a COS/MOS integrated circuit.

As the initial step in the formation of a COS/MOS IC, p-type material is diffused vertically into the n-type substrate to form p-type regions (p-wells) in which the n-channel MOS devices will be located. This initial step is shown in Fig. 11. Low-resistance p^+-type pockets, such as those shown in Fig. 12, are diffused into the n-type substrate to form the source and drain regions of the p-channel devices

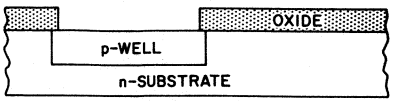


Fig. 11 — Formation of p-type regions in which n-channel MOS devices will be located.

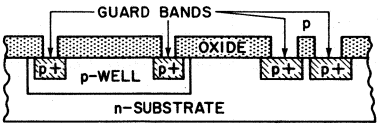


Fig. 12 — Low-resistance p^+-type pockets in the n-type substrate.

and guard bands for n-channel devices. Low-resistance n^+-type pockets, like those shown in Fig. 13, are diffused into the p-well regions to form the source and drain regions of

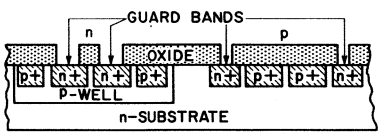


Fig. 13 — Low-resistance n^+-type pockets in the p-well region.

the n-channel devices and guard bands for p-channel devices. A detailed explanation of guard bands is given in the subsequent discussions on **COS/MOS Design and Layout.** (The gate-protection network is described in detail in the subsequent section on **Basic Building Blocks for COS/MOS Integrated Circuits.)**

As has been described, silicon dioxide (SiO_2) is necessary in integrated-circuit processing as a diffusion mask. However, in MOS processing, SiO_2)plays an additional and more important role as a dielectric used to cover the channel region

and insulate it from the metal gate. The processing technology by means of which a suitable oxide layer is obtained is the key to fabricating MOS devices.

It has been found that SiO_2 usually contains some ion contamination (most often sodium ions), and that these ions are positively charged. The positive charge carried by the ions can affect the characteristics of MOS devices significantly. In many instances this charge is fixed; in others, it is movable when stressed with voltage at elevated temperatures. The presence of a movable charge is very undesirable because it can cause serious problems in device stability and reliability. Therefore, **clean-oxide** technology has been developed to eliminate the contamination. This technology has made possible the fabrication of reliable n-channel and p-channel enhancement devices and thus is responsible for the development of the complementary-symmetry arrangement in integrated MOS devices.

Another important use of SiO_2 in MOS integrated circuits is as a **field oxide**, a thick oxide that insulates all non-active regions of the MOS IC from the interconnection metal. This insulation is needed to raise the threshold voltage of the inactive regions to a level beyond the operating voltage of the system so that undesired leakage currents are eliminated. The threshold voltage of the field oxide is usually referred to as the field threshold voltage.

Metallization of Completed Wafers

The series of oxidation and diffusion operations culminates in an integrated-circuit wafer that contains the desired electronic elements. High-conductivity metallic paths are then needed to interconnect these elements. The process by which these paths are fabricated is called metallization.

The **metallization** process is comprised of metal deposition, interconnection pattern delineation, and alloying. Metal deposition is performed by placing the processed wafer in a vacuum of about 10^{-6} torr (10^{-9} atmosphere). The source material (usually aluminum), which is also in the vacuum chamber, is then heated above its vaporization point by means of induction or resistance heating techniques. As a result, metal is released by vaporization and condensed on the integrated-circuit wafer, coating it completely to a controlled thickness. The metal-coated wafer is then subjected to photolithographic procedures, including application of photoresist lacquer, exposure to ultraviolet light through a photomask having the desired pattern, and the removal of unwanted metal by acid etching. The resulting interconnection patterns are similar to that shown in Fig. 14. Finally, in order to assure excellent electric contact between the aluminum and the electronic elements, the metallized wafers are heated in a furnace for a controlled period to permit a slight alloying of the aluminum with the semiconductor junctions.

As shown in Fig. 10, the metallic interconnections terminate at the edges of the integrated-circuit chip as pads to which very fine wires connect the chip to the package terminals as shown in Fig. 14.

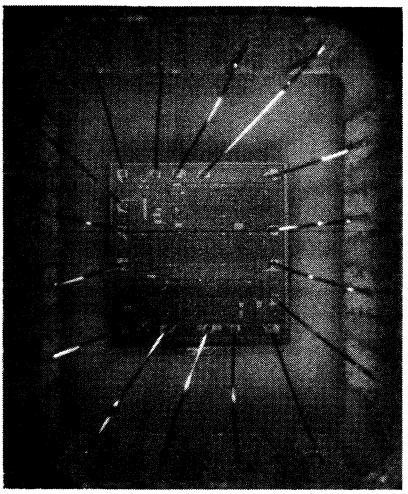


Fig. 14 – Integrated-circuit chip mounted with chip connected to package terminals.

Probe Testing of Metallized Wafers

Elaborate automatic equipment has been developed to test chips while they are constituents of a complete wafer. The test procedure is frequently called "**wafer-probing.**" A large number of needle-tipped probes make simultaneous electrical contact with the aluminum electrode pads on each chip. The probing equipment is designed so that the wafer is indexed automatically, with the probes contacting the individual chips sequentially.

Assembly and Final Testing

After the probe testing of the wafer is completed, the individual circuit chips must be separated and assembled into integrated-circuit packages. The packaged devices are then subjected to hermeticity, environmental, and final electrical testing. The sequence of events employed for these operations is as follows:

Separation of Chips – The individual chips in a wafer are separated by a technique similar to that used in glass cutting. A fine diamond point is used to "scribe" the wafer with its constituent chip pattern. The actual separation into chips is accomplished by an operation called "dicing," which is simply a system of mechanical fixturing by which stress is applied to the wafer in such a manner that mechanical separations occur along the scribed lines. "Sorting" is the rejection of chips which were found to be defective in wafer-probing or dicing operations. Microscopic inspection of each chip is performed to cull out circuits with visible imperfections.

Chip Bonding – In this procedure, the chip is securely mounted in the package by means of a silver-filled conductive epoxy.

Lead Bonding – After the chip is firmly affixed in the package, electrical connections are made to the terminal-post leads. Aluminum wires of about 1.5-mil diameter are commonly used to make these connections.

Capping and Sealing – The lead-bonded header is usually subjected to cleaning and vacuum bake-out operations prior to sealing. Actual hermetic sealing is accomplished by a variety of means, depending to some extent on the package design. Local application of heat (e.g., welding) is used to seal the cap to the package header. This step is conducted in a dry atmosphere. In the case of non-hermetic packages like plastic, the lead-bonded chip assembly is

encapsulated in plastic or epoxy materials.

Hermeticity and Environmental Testing – Hermeticity testing is used to confirm the leak resistance of the package. The helium leak-detection technique is frequently used. In this method, completed packages are placed in an atmosphere of helium pressure for a period of time. Helium is able to penetrate through any imperfections which may exist in the package. After removal from the helium pressurization chambers, sensitive mass-spectrograph leak detectors are used to detect helium "oozing" out of any imperfection in the package.

Mechanical shock, vibration, acceleration, and thermal shock testing are used to screen out devices which have inadequate margins against anticipated stresses for the particular class of service in which the integrated circuit is to be applied.

Final Electrical Testing – Wafer-probing of COS/MOS integrated-circuit chips is usually limited to static parameter tests and dc functional tests because the length of probe leads and other factors prevent meaningful ac, rf, or pulse testing. Consequently, any ac testing required is performed on packaged units only. Test equipment presently used on COS/MOS integrated circuits is almost entirely automated.

COS/MOS DESIGN AND LAYOUT

COS/MOS integrated circuits are normally fabricated on an n-type substrate which serves as the substrate material for all p-channel MOS devices as well as p^+ tunnels, diodes, and resistors. A p-type substrate is provided for the complementary n-channel MOS devices, n^+ tunnels, diodes, and resistors by diffusion of a lightly doped p-well region into the original n-type substrate as described previously in the paragraphs concerning **COS/MOS IC Wafer Processing.** The n-channel units exhibit the higher carrier mobility associated with electrons; they have approximately twice the transconductance of p-channel units with identical geometry. Therefore, the matching of a p-channel with an n-channel unit requires that a p-channel unit with a given channel length L have approximately twice the channel width W of the n-channel unit with which it is to be matched.

Guard Bands

Protective **guard bands** surround separate MOS devices, tunnels, wells, and diodes or combinations of MOS devices which are interconnected through common diffused regions for the purpose of preventing leakage between the entities named. All p-channel devices, tunnels, and diodes must be surrounded by a continuous n^+ guard band which also serves as a tunnel to help conduct current from the external supply voltage V_{DD} across the n-type substrate to every p-channel device tied to the external supply. Similar heavily doped p^+ guard bands surround all n-channel devices, tunnels, and diodes to help conduct current from the external ground supply V_{SS} across the p-well to every n-channel device tied to ground. Contact to the n-type substrate may be made through the n^+ guard band and

returned to the V_{DD} pad; contact to the p-well substrate may be made through the p^+ guard band and returned to the ground pad. Fig. 15 illustrates a typical p- and n-channel MOS complementary pair with appropriate connections to V_{DD} and V_{SS}, respectively. Fig. 16 is a cross section of the complementary pair of Fig. 15 showing the use of n^+ and p^+ guard bands for interconnecting the source regions to the V_{DD} and V_{SS} pads, respectively. Guard bands may be narrow strips or, where space permits, large diffused areas that minimize resistance in the V_{DD} and V_{SS} supply lines. Guard bands are also used to assure positive device cutoff; this cutoff is accomplished by having the gate metal, as it leaves the

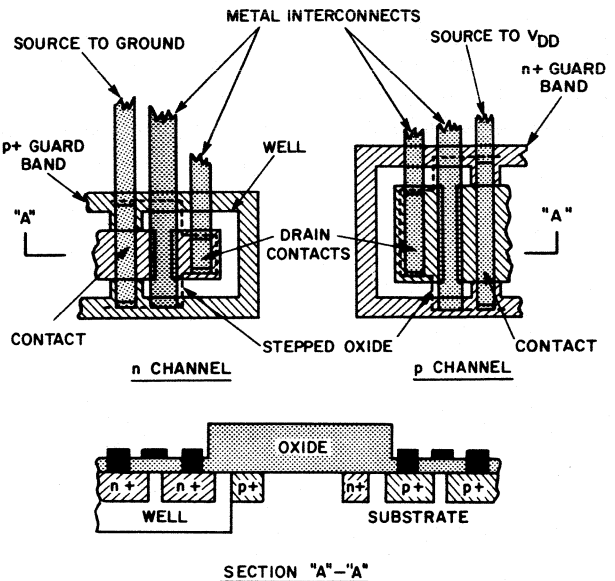


Fig. 15 — Plan and cross-sectional views of a typical MOS complementary-transistor pair.

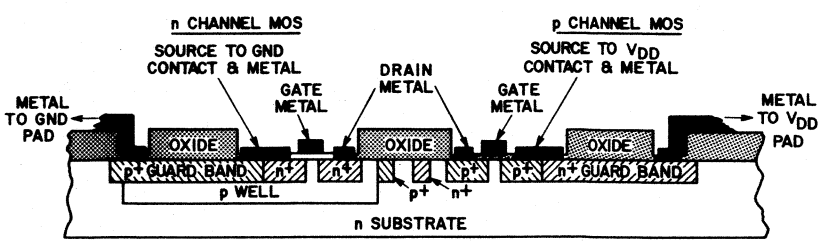


Fig. 16 — A cross section of the complementary pair of Fig. 15 showing the use of guard bands.

end of the channel, cross a guard band prior to stepping up over the thick oxide as shown in Fig. 16.

Typical Inverter and Logic Gate Layout

A typical layout for the basic COS/MOS inverter circuit is shown in Fig. 17. The figure shows the single n-channel MOS transistor and its complementary p-channel counterpart with the gates and drains tied to each other and with metal interconnects between source and V_{SS} and source and V_{DD}, respectively.

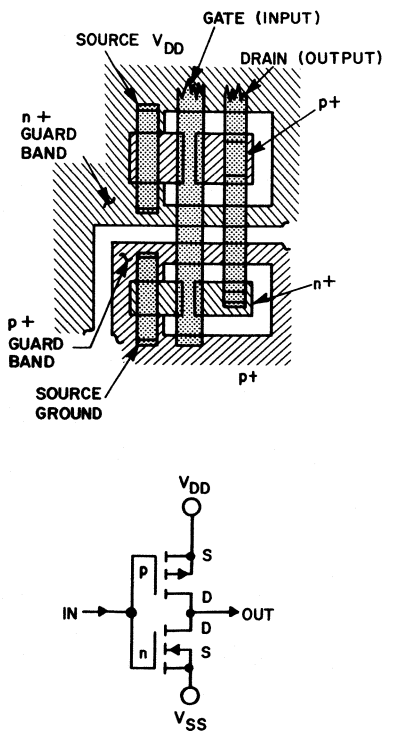


Fig. 17 – Typical layout and circuit diagram for the basic COS/MOS inverter circuit.

The basic inverter may be extended, as described in the section on **Basic Building Blocks for COS/MOS Integrated Circuits**, to true complementary logic. The logical NOR gate is formed by placing the n-channel units in parallel and the p-channel units in series. Figs. 18 and 19 illustrate 2- and 3-input NOR gates. In the figures, the source-to-V_{DD} and source-to-V_{SS} connections are made to the n^+ and p^+ guard

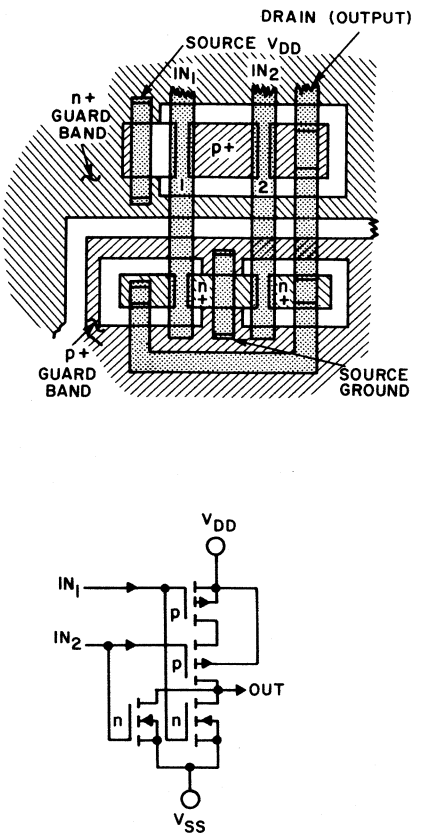
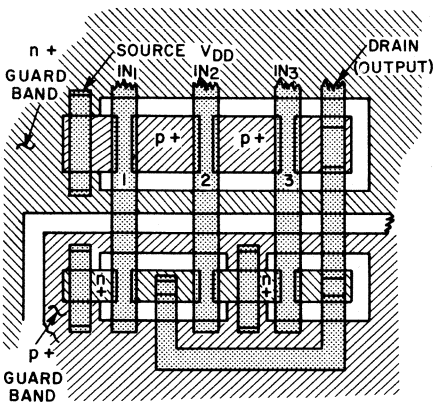


Fig. 18 – Typical layout and circuit diagram for a 2-input NOR gate.

bands because these guard bands are tied directly to V_{DD} and ground, respectively. Variations of these layouts are used in the CD4000A dual 3-input gate and CD4001A quad 2-input gate. If the above arrangement



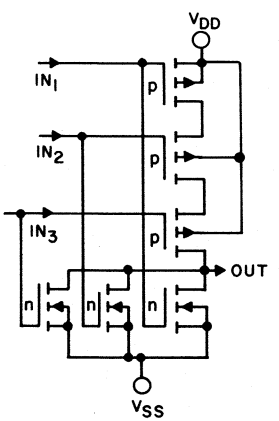


Fig. 19 – Typical layout and circuit diagram for a 3-input NOR gate.

is reversed, i.e., if the p-channel units are placed in parallel and the n-channel units in series, NAND gates result, as in the CD4011A quad 2 and CD4012A dual 4-input NAND gate circuits.

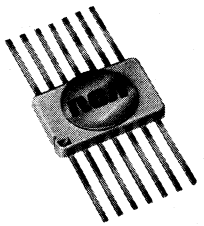
PACKAGES

RCA COS/MOS integrated circuits are currently packaged in three distinct configurations: the TO-5-style glass-metal package, the ceramic flat pack, and the dual-in-line package. The dual-in-line package may be either ceramic or plastic. The TO-5-style package has 12 leads; the flat pack and the dual-in-line packages have 14, 16, or 24 leads. Fig. 15 shows the different types of integrated-circuit packages and the JEDEC type number designations for them.

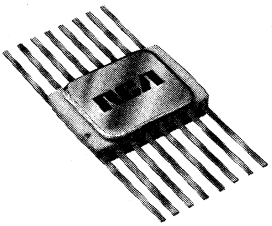
The letters D, E, K, and T appended to a device identification identify the type of package in which the device is enclosed.

Designation	Meaning	Standard Pins Available
E	Dual In-Line Plastic	14,16
D	Dual In-Line Ceramic	14,16,24
K	Flat Pack	14,16,24
T	TO-5 Package	12

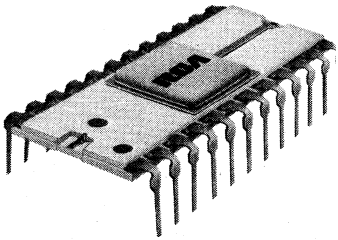
For example, a CD4006AK is a CD4006A circuit in a ceramic flat pack, a CD4006AD is a CD4006A circuit in a dual in-line ceramic package, and the CD4006AE is the CD4006A circuit in a dual in-line plastic package.



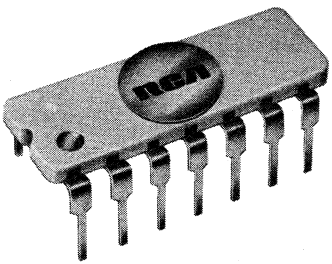
14-Lead
Flat Pack
(JEDEC MO-004-AF)



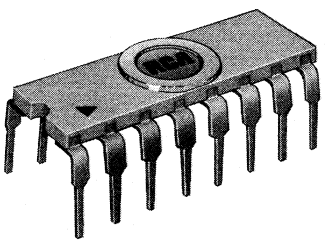
16-Lead
Flat Pack
(JEDEC MO-004-AG)



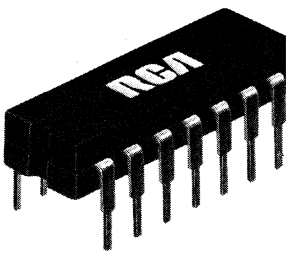
24-Lead Dual-in-
Line Ceramic
(JEDEC MO-015-AG)



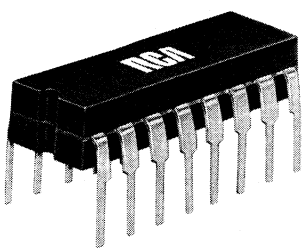
14-Lead Dual-in-
Line Ceramic
(JEDEC MO-001-AD)



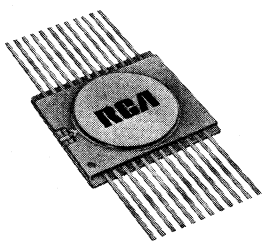
16-Lead Dual-in-
Line Ceramic
(JEDEC MO-001-AE)



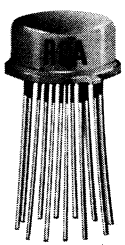
14-Lead Dual-in-
Line Plastic
(JEDEC MO-001-AB)



16-Lead Dual-in-
Line Plastic
(JEDEC MO-001-AC)



24-Lead
Flat Pack



12-Lead
TO-5-Style

Fig. 20 – RCA COS/MOS IC packages.

Basic Building Blocks for COS/MOS Integrated Circuits

This section describes several circuits (building-block units) that form the basis for the more complex circuits discussed later in the Manual. The input-protection circuitry incorporated into each RCA COS/MOS integrated circuit is also described. Because COS/MOS IC's are particularly well suited for digital applications, the basic circuits are described from that point of view.

INVERTER

The most basic of all the COS/MOS circuits, the **inverter** circuit, consists of one p-channel and one n-channel enhancement-type MOS transistor, as shown in Fig. 21. The substrate of the p-channel device is at $+V_{DD}$, and the substrate of the n-channel device is at ground. Consequently, when the voltage at the input of the inverter is zero (logic 0), the input is at $-V_{DD}$ relative to the substrate of the p-channel device and at zero volts relative to the substrate of the n-channel device. The result is that the p-channel

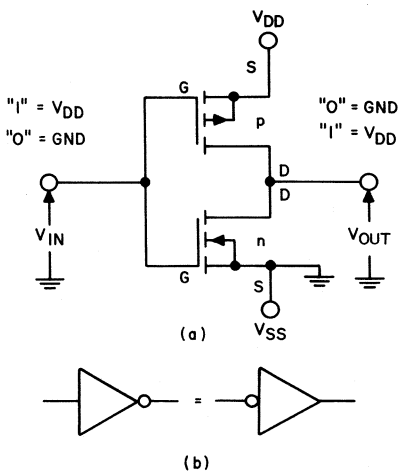


Fig. 21 – COS/MOS inverter circuit: (a) schematic diagram; (b) logic diagrams.

device is turned on and the n-channel device is turned off. Under these conditions, there is a low-impedance path from the output to V_{DD}, and a very-high-impedance path from the output to ground; therefore, the output voltage approaches V_{DD} (logic 1) under normal loading conditions. When the input voltage is $+V_{DD}$ (logic 1), the situation is

reversed: the p-channel unit is OFF and the n-channel unit is ON (i.e., $V_{GS} = V_{DD}$) with the result that the output voltage approaches zero (logic 0).

In either logic state, one MOS transistor is ON while the other is OFF. Because one transistor is always turned off, the quiescent power consumption of the COS/MOS unit is extremely low; more precisely, it is equal to the product of the supply voltage and the leakage current (i.e., $P_D = V_{DD}I_L$).

The process of creating the source-drain and p-well diffusions for the inverter circuit, as shown in Fig. 22(a), also creates parasitic diodes which are connected to the basic inverter nodes, as shown in Fig. 22(b). These parasitic elements (D_1, D_2, and D_3) are back-biased across the power supply and contribute in part to the device leakage current and thus to the quiescent dissipation. Additional diodes are also diffused into the over-all structure, as shown in Fig. 22(b), to form an input limiter circuit that provide protection against static voltages. Any gate input node that is brought out to a package terminal is protected by this network. The operation of the input protection circuit is described in the section on **Basic Building Blocks for COS/MOS Integrated Circuits.**

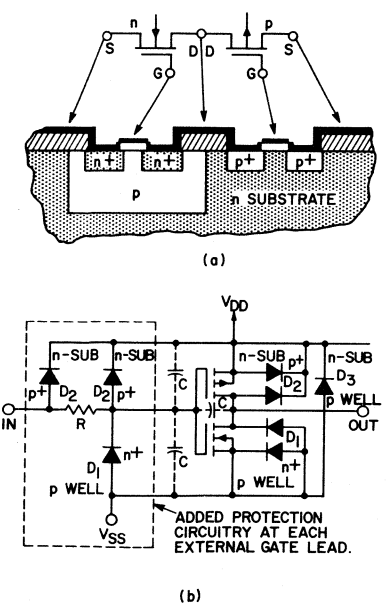


Fig. 22 – (a) Cross section of inverter-circuit chip showing parasitic diodes; (b) connection of the diodes to basic inverter nodes.

RCA COS/MOS products range from circuits as simple as 2-input **logic gates** through the complexity of a 64-stage shift register. These devices are composed of varying numbers of interconnected inverter circuits placed on silicon chips of varying area. Therefore, the leakage current ranges widely because it depends on the number of interconnected circuits and the parasitic diode area associated with each circuit. For example, the dissipation of a logic gate (the CD4001) is typically 0.01 microwatt at 10 volts, while the dissipation of the 64-stage shift register (CD4031) is typically 10 microwatts at 10 volts, even though both of these device types are processed similarly.

Device Switching Characteristics

Because of the complementary nature of the interconnections of the series p- and n-type devices in the basic inverter, the **transfer characteristic** of a COS/MOS logic gate is as shown in Fig. 23. The high input

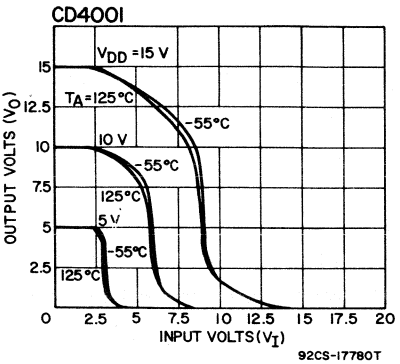


Fig. 23 — Transfer characteristic of a COS/MOS logic gate.

impedance of the gate results in no dc loading on the output so that the input and output signals are allowed to swing completely from zero volts (logic 0) to V_{DD} (logic 1) when sufficient time settling is allowed. The switching point is shown to be typically 45 to 50 per cent of the magnitude of the power-supply voltage, and varies directly with that voltage over the entire range of supply voltage specified for COS/MOS devices. The COS/MOS transfer characteristic of Fig. 23 illustrates the high noise immunity of COS/MOS devices; i.e., typically 45 per cent of the supply voltage. Fig. 23 also shows the negligible change in operating point as temperature ranges from -55°C to +125°C. Because of the ideal nature of these switching characteristics, COS/MOS devices operate reliably over a much wider range of voltage than other forms of logic circuits.

AC Dissipation Characteristics

All significant COS/MOS power dissipation is ac in nature and is a direct function of load capacitance C, operating supply voltage V, and switching rate f.

During the transition from a logical 0 to a logical 1, both transistors in the COS/MOS inverter are momentarily ON with the result that, instantaneously, a pulse of current is drawn from the power supply. The magnitude of this current depends on the impedance and threshold voltage of the inverter transistors, as well as the magnitude of the power-supply voltage and the length of time spent in transition (e.g., the input rise or fall time). Current is also required to charge and discharge the output load capacitance. The dissipation that results from the current components described above is directly proportional to the frequency of operation and amount of capacitive loading and may be expressed as follows:

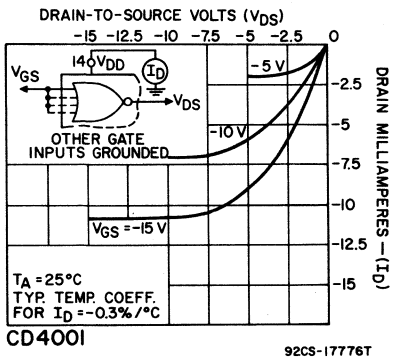
$$P_{ac} = CV^2f \qquad (13)$$

The more often the circuit switches, the greater the current; the heavier the capacitive loading, the greater the resultant dissipation.

AC Performance Characteristics

As indicated above, the node capacitances located within or external to a given circuit are charged and discharged during switching through the channel resistance of the p- or n-type device. As the magnitude of V_{DD} increases, the impedance of the conducting channel decreases; this nonlinear property of MOS devices can be observed from a close scrutiny of the characteristic curves

shown in Fig. 24. The result of the increase in channel conductivity is that the maximum switching speed



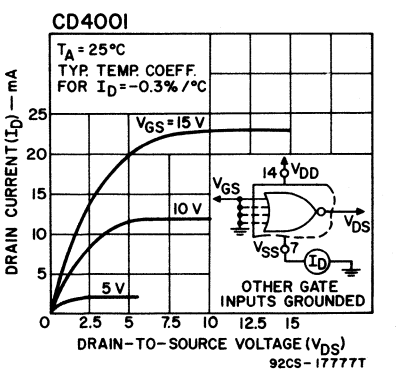
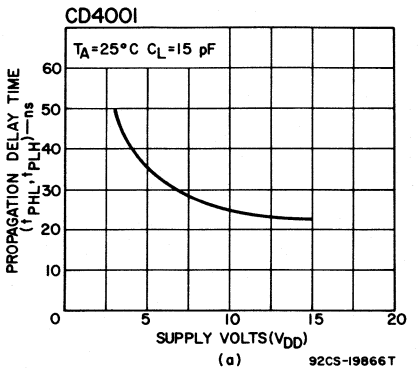


Fig. 24 — Curves demonstrating the decrease in conducting-channel impedance with increase in V_{DD}.

of COS/MOS devices increases with increasing supply voltage as shown in Fig. 25(a). The effect of increasing external load capacitance is shown in Fig. 25(b).



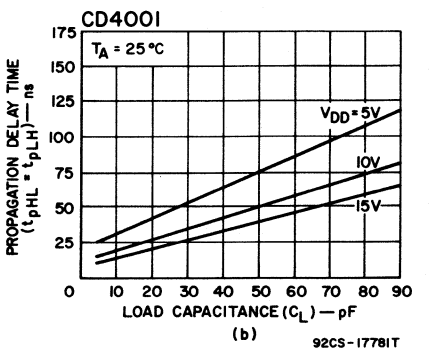


Fig. 25 — (a) Curve illustrating increase in maximum switching speed with decrease in channel conductivity; (b) effect on switching speed of increasing external load capicitance.

TRANSMSSION GATES

The COS/MOS transmission gate is a single-pole, single-throw switch formed by the parallel connection of a p-type and an n-type device. This switch expands the versatility of COS/MOS circuits in both digital and linear applications.

The perfect transmission gate or switch may be characterized as having zero forward and reverse resistance when closed and infinite

resistance when open; i.e., it has an infinite OFF/ON impedance ratio. The COS/MOS transmission gate approaches these ideal conditions.

The advantages of a COS/MOS transmission gate can be better understood by consideration first of the single n-channel MOS-transistor transmission gate driving a capacitive load from a positive voltage source, as shown in Fig. 26. With 0 volts applied to the gate of the n-channel device, no current can flow, and the

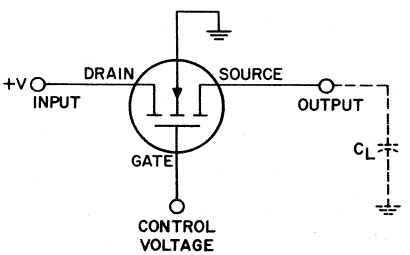


Fig. 26 – Single n-channel MOS-transistor transmission gate.

load capacitance C_L remains uncharged. As the gate voltage to the transmission gate is made positive enough to turn the transmission gate on, however, the load capacitance begins to charge. However, the load capacitance can only charge to a level equal to the gate voltage minus the threshold voltage of the n-channel transistor because the single n-channel transmission gate operates as a source-follower circuit in which premature gate cutoff occurs. Another aspect of MOS transmission gates is that they are bilateral; i.e., drain and source are interchangeable. This type of transmission gate also operates with slow speed in large-signal applications; i.e., as the device begins to turn on, the RC time constant is large. A COS/MOS transmission gate which overcomes these disadvantages is made by paralleling n- and p-channel MOS transistors as shown in Fig. 27. This arrangement

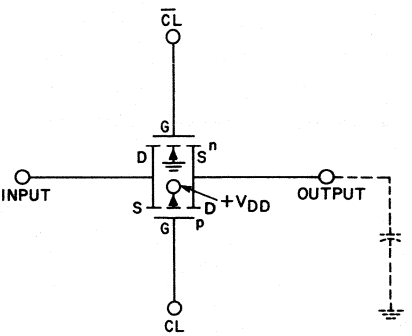


Fig. 27 – COS/MOS transmission gate.

overcomes the premature-cutoff problem associated with the single-channel transmission gate because one of the two channels is always being operated as a drain-loaded stage regardless of what the input or output voltage may be. If each MOS channel of the COS/MOS circuit has a 2-volt threshold voltage and if 0 volts is applied to the gate of the p-channel unit and 10 volts to the gate of the n-channel unit, an increase in input voltage in excess of 8 volts (10 volts – 2 volts) cannot be switched through the n-channel unit. However, proper switching can occur in the p-channel unit because the magnitude of the voltage from gate to source (0 volts – 8 volts = -8 volts) is greater than the p-channel threshold (-2 volts). As a result, the switch does not turn off prematurely because the gate-to-source voltages of both the n- and p-channel units never equal the threshold voltages of these

devices. The full 10-volt supply voltage (V_{DD} - V_{SS} = 10 volts) can, therefore, be switched. The COS/MOS transmission gate is also considerably faster than the single-channel MOS transmission gate; the RC time constant is always smaller.

The transmission gate can be combined with a basic inverter circuit to form a single switch as shown in Fig. 28. Only one control voltage is required because the inverter provides the control voltage necessary for the complementary unit. The circuit of Fig. 28 is useful in a variety of analog and digital multiplexing applications.

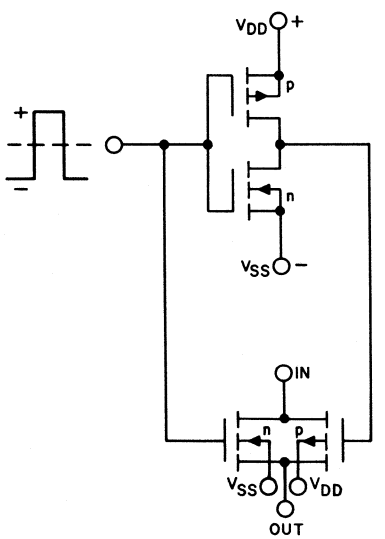


Fig. 28 – Combination of transmission gate and basic inverter to form a switch.

TRANSMSSION GATE AND INVERTER APPLICATIONS

At present, all COS/MOS integrated circuits are constructed of two basic building blocks, the inverter and the transmission gate. The basic inverter forms all the NOR and NAND gates. Combined with transmission gates, the inverter forms more complicated circuits, such as flip-flops, counters, shift registers, arithmetic blocks, and memories.

NOR Gates

A two-input **NOR gate** is an inverter with two n-type units in parallel and two p-type units in series, as shown in Fig. 29. Each of the two inputs is connected to the gate of one n- and one p-channel transistor. A negative output is obtained when either the A or the B input is positive because the positive input turns off the associated p-channel transistor, disconnecting the output from the V_{DD} supply, and turns on the associated n-channel transistor, connecting it to ground and causing a low output. When both of the input signals are at ground potential, both p-channel units are on and both n-channel units off. In this case the output is coupled to the V_{DD} terminal and provides a high output. Three- and four-input NOR gates may be formed by placing three or four n-channel transistors in parallel and three or four p-channel transistors in series in an arrangement similar to that shown in Fig. 29.

NAND Gates

A NAND gate is an inverter with two p-channel transistors in parallel, and two n-channel transistors in series, as shown in Fig. 30. The output goes negative only if both inputs are positive, in which case the

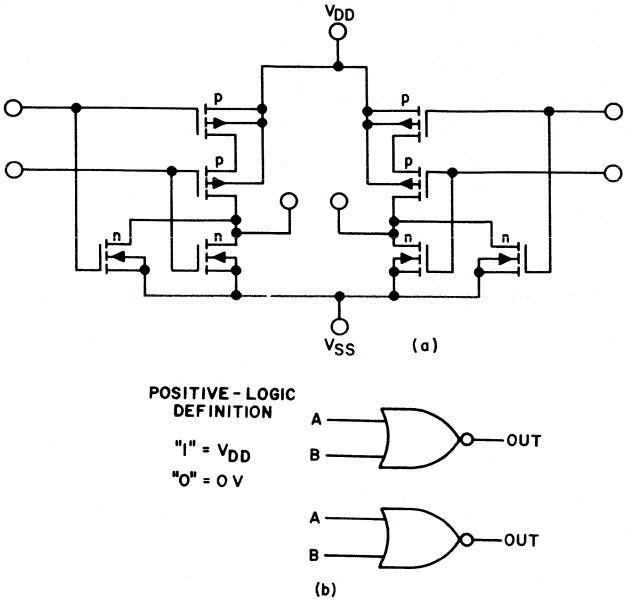


Fig. 29 — A pair of two-input NOR gates: (a) schematic diagram; (b) logic diagram.

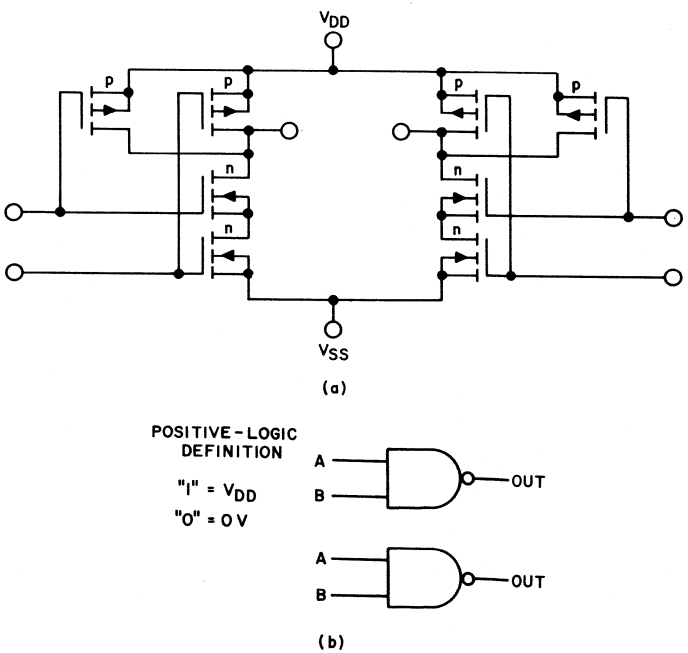


Fig. 30 — A pair of NAND gates: (a) schematic diagram; (b) logic diagram.

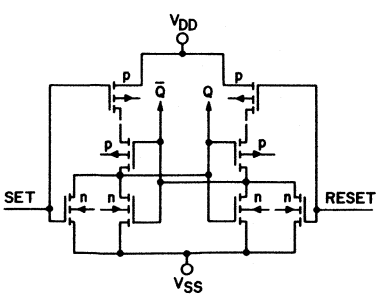
p-channel transistors are turned off and the n-channel transistors on. This condition couples the output to ground. If either input is negative, the associated n-channel transistor is turned off, and the associated p-channel transistor on; thus the output is coupled to V_{DD} and goes high. Again, three- or four-input NAND gates may be formed by placing three or four p- and n-channel transistors in parallel and in series, respectively, in an arrangement similar to that shown in Fig. 30.

Set-Reset Flip-Flops

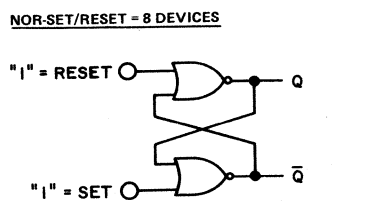
Two NOR gates may be connected as shown in Fig. 31 to form a **set-reset flip-flop**. When the set and reset inputs are low, one amplifier output is low, and the other high, and there is a stable condition. If the set input is raised to a higher level, the associated n-channel unit is turned on so that the output of the set stage goes high and becomes logic 1 or $\overline{Q}$. Under these conditions the flip-flop is said to be in the SET state. Raising the reset input level causes the other output to go high, and places the flip-flop in the RESET state (Q represents the low output state). Thus, the circuit of Fig. 31 represents a static flip-flop with SET and RESET capability.

D Flip-Flops

A block diagram of a **D-type flip-flop** is shown in Fig. 32(a); the schematic diagram for the flip-flop is shown in Fig. 32(b). The block diagram shows a master flip-flop formed from two inverters and two transmission gates (shown as switches) that feeds a slave flip-flop having a similar configuration. When the input signal is at a low level, the TG_1 transmission gates are closed and the TG_2 gates open. This configuration allows the master flip-flop to sample incoming data, and the slave to hold the data from the previous input and feed it to the output. When the clock is high, the TG_1 transmission gates open and the TG_2 transmission gates close, so that the master holds the data entered and feeds it to the slave. The D flip-



(a)



TRUTH TABLE

SET	RESET	Q	Q̄	
1	0	1	0	
0	1	0	1	
1	1	0	0	
0	0	Q	Q̄	NO CHANGE

(b)

Fig. 31 – Set/reset flip-flop: (a) schematic diagram; (b) logic diagram and truth table.

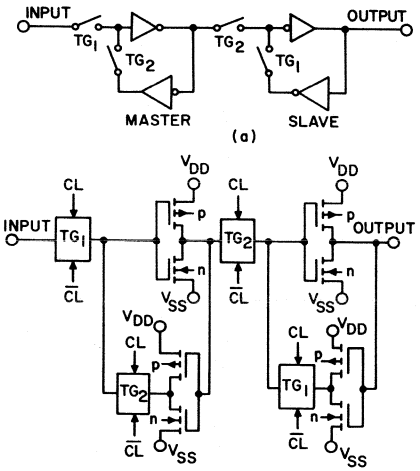


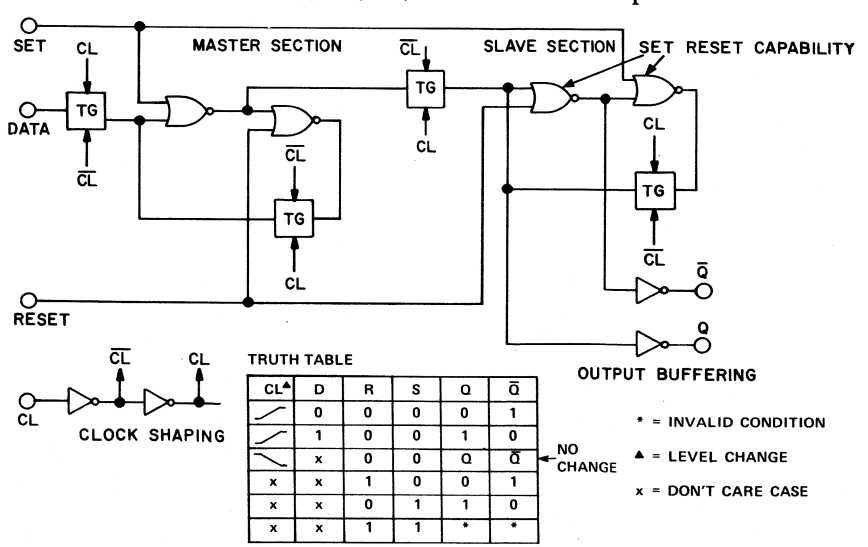
Fig. 32 — (a) Block, (b) schematic, and (c) clock-pulse diagrams for a D-type flip-flop.

flop is static and holds its state indefinitely if no clock pulses are applied, i.e., it stores the state of the input prior to the last clocked input pulse. A **clock pulse** is the pulse applied to the logical elements of a sequential digital system to initiate logical operations. Both the "clock", CL, and "inverted clock", $\overline{CL}$, as shown in Fig. 32(c), are required; clock inversion is accomplished by an inverter internal to each D flip-flop.

Fig. 33 shows the logic diagram and truth table for a D-type flip-flop.

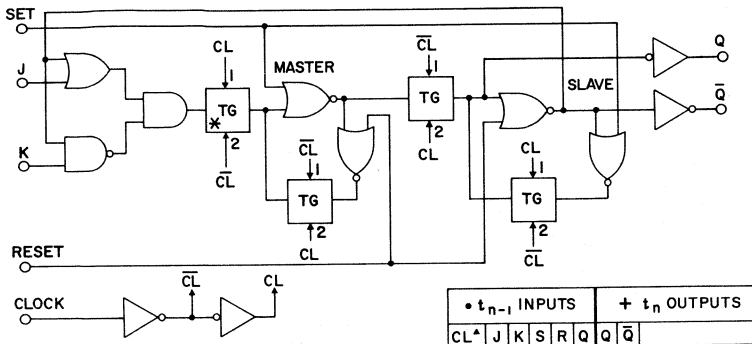
J-K Flip-Flops

The logic diagram and "truth" table for a J-K flip-flop is shown in Fig. 34. The J-K flip-flop is similar in some respects to the D flip-flop, but has some additional circuitry to accommodate the J and K inputs. The J and K inputs provide separate clocked set and reset inputs, and allow the flip-flop to change state on successive clock pulses.

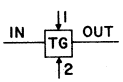


CL▲	D	R	S	Q	$\overline{Q}$
⌒	0	0	0	0	1
⌒	1	0	0	1	0
⌣	x	0	0	Q	$\overline{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	*	*

Fig. 33 — Logic diagram and "truth" table for a D-type flip-flop.



* – TG = TRANSMISSION GATE: INPUT TO OUTPUT IS A BIDIRECTIONAL SHORT CIRCUIT WHEN CONTROL INPUT 1 IS LOW AND CONTROL INPUT 2 IS HIGH; AN OPEN CIRCUIT WHEN CONTROL INPUT 1 IS HIGH AND CONTROL INPUT 2 IS LOW.



+ – t_n REFERS TO THE TIME INTERVALS AFTER THE POSITIVE CLOCK PULSE TRANSITION.

• t_{n-1} INPUTS						+ t_n OUTPUTS		
CL▲	J	K	S	R	Q	Q	$\bar{Q}$	
↗	1	X	0	0	0	1	0	
↗	X	0	0	0	1	1	0	
↗	0	X	0	0	0	0	1	
↗	X	1	0	0	1	0	1	
↘	X	X	0	0	X			←(NO CHANGE)
X	X	X	1	0	X	1	0	
X	X	X	0	1	X	0	1	
X	X	X	1	1	X	*	*	

▲ – LEVEL CHANGE
X – DON'T CARE
* – INVALID CONDITION
• – t_{n-1} REFERS TO THE TIME INTERVAL PRIOR TO THE POSITIVE CLOCK PULSE TRANSITION.

Fig. 34 – Logic diagram and "truth" table for a J-K flip-flop.

The J-K flip-flop circuit also has set and reset capability; the inverters in the master and slave flip-flop each have an added OR input for direct (unclocked) setting and resetting of the flip-flop.

Memory Cells

The basic storage element common to all RCA COS/MOS memories consists of two COS/MOS inverters cross-coupled to form a flip-flop as shown in Fig. 35. Single-transistor transmission gates are employed as a simple and efficient means of performing the logic functions associated with storage-cell selection; i.e., the sensing and storing operations. The resulting word-organized storage cell, shown in Fig. 36, is composed

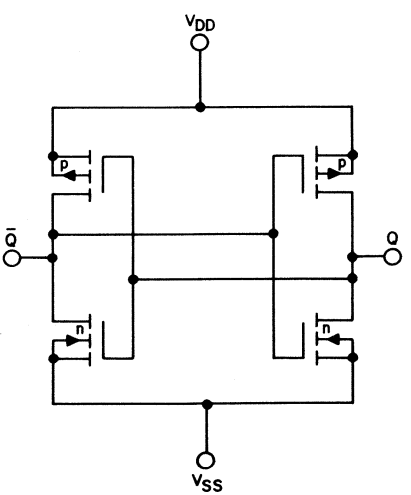


Fig. 35 – The basic storage element common to all RCA COS/MOS Memories.

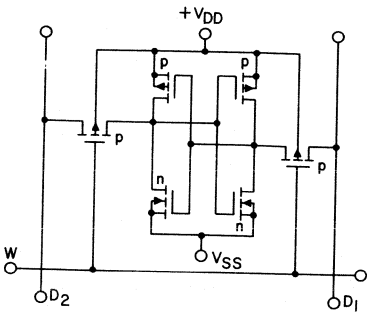


Fig. 36 – A word-organized storage cell: W is word line, D_1 and D_2 are data lines.

of six transistors; one word line, W; and two digit-sense lines, D_1 and D_2. Addressing is accomplished by energizing a word line; this action turns on the transmission gates on both sides of the selected flip-flop. Because the cell in Fig. 36 has p-channel transmission gates, a ground-level voltage is required for selection. Fig. 37 shows an 8-transistor bit-organized memory cell employing X-Y selection. A modification of this circuit in which the Y-select transistors are common for each column of storage elements is used in large memory arrays.

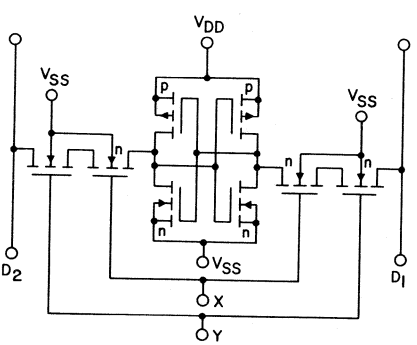


Fig. 37 – Eight-transistor bit-organized memory cell with X-Y selection.

Dynamic Shift Registers

Fig. 38(a) shows a two-stage **shift register**; each stage consists of two inverters and two transmission gates. Each transmission gate is driven by two out-of-phase clock signals arranged, as shown in Fig. 38(b), so that when alternate transmission gates are turned on, the others are turned off. When the first transmission gate in each stage is turned on, it couples the signal from the previous stage to the inverter, and causes the signal to be stored on the input capacitance to the inverter. The shift register utilizes the input of the inverter for temporary storage.

When the transmission gate is turned off on the next half cycle of the clock, the signal is stored on this input capacitance, and the signal remains at the output of the inverter where it is available to the next transmission gate, which is now turned on. Again, this signal is applied to the input of the next inverter where it is stored on the input capacitance of the inverter, making the signal available at the output of the stage. Thus a signal progresses to the right by one half stage on each half cycle of the clock, or by one stage per clock cycle.

Because the shift register is dependent upon stored charge which is subject to slow decay, there is a minimum frequency at which it will operate; reliable operation can be expected at frequencies as low as 5 kHz.

COS/MOS dynamic shift registers have all the advantages of other COS/MOS devices including low power dissipation, high noise immunity, and wide operating voltage

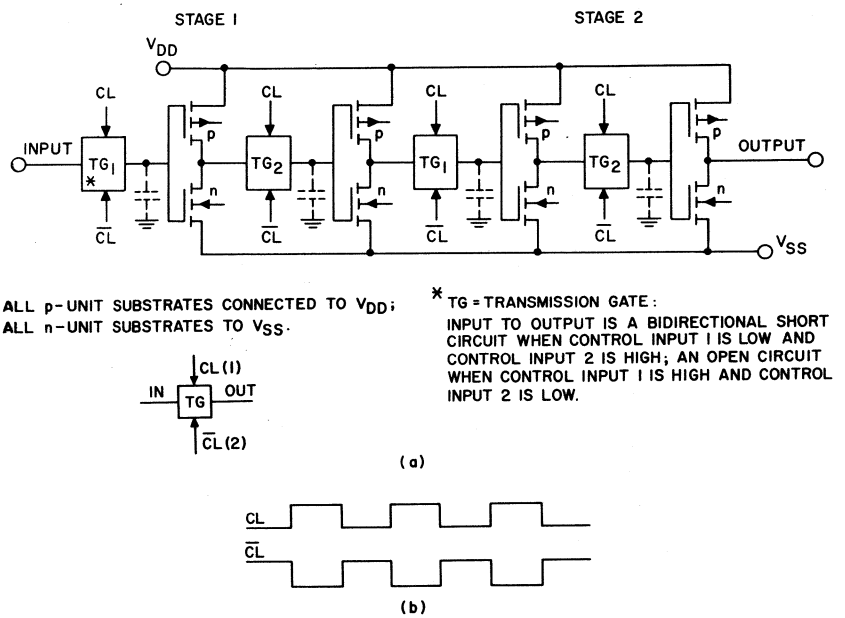


Fig. 38 – (a) Two-stage shift register; (b) clock-pulse diagram.

range and, in addition, are superior in two important ways to the single-channel (p-MOS and n-MOS) dynamic shift registers. First, the COS/MOS device easily generates the two-phase clock signals required internal to itself with just one supply voltage. Second, TTL and DTL logic compatibility is maintained on all inputs and outputs with one supply voltage.

INPUT PROTECTION

The standard **input protection** device used in all RCA COS/MOS IC's is shown in Fig. 39. Protection is required to prevent damage to the MOS input gates that could result from careless handling and/or testing prior to final installation. Fig. 39 illustrates the positive, built-in protection afforded by the diode

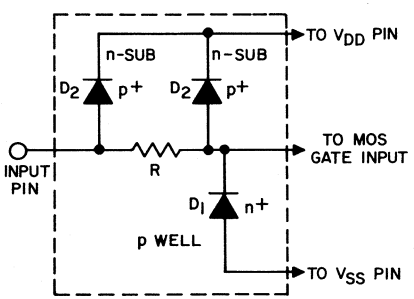
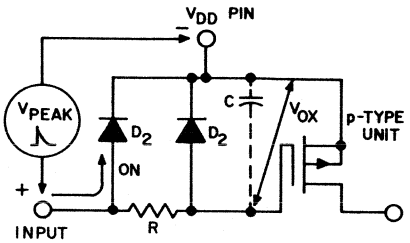


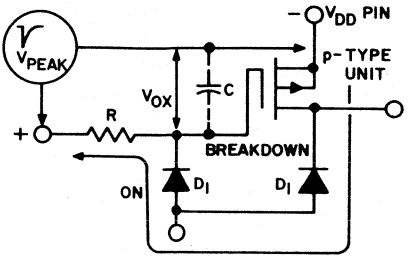
Fig. 39 – COS/MOS-IC protection circuit showing diode clamps.

clamps in a COS/MOS circuit; this approach is in contrast to the widely varying zener-diode breakdown protection used in bipolar circuits. Fig. 40 shows several diode-clamp schemes that may be used to provide input protection for different operating conditions.



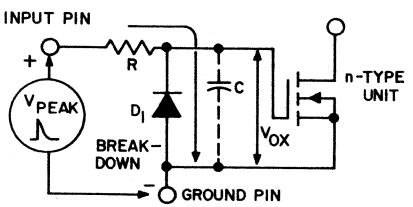
$V_{OXIDE\ MAX} = V_{D2}$ FORWARD ≤ 1 V ON CONDUCTION
p-TYPE UNIT

(a)



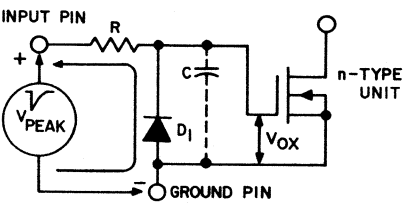
$V_{OXIDE\ MAX} = V_{DI}$ (ON) + V_{DI} (BREAKDOWN) + p-TYPE UNIT (ON)
= 1 V + 25 V + 4 V = 30 V
p-TYPE UNIT

(b)



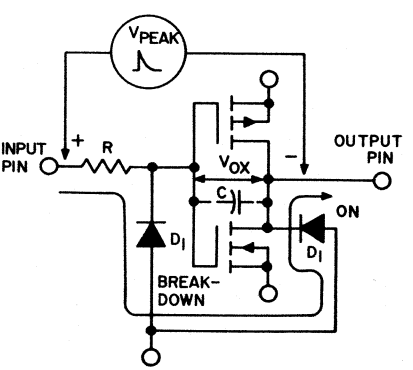
$V_{OXIDE\ MAX} = V_{DI\ BREAK-DOWN} = 25$ V
n-TYPE UNIT

(c)



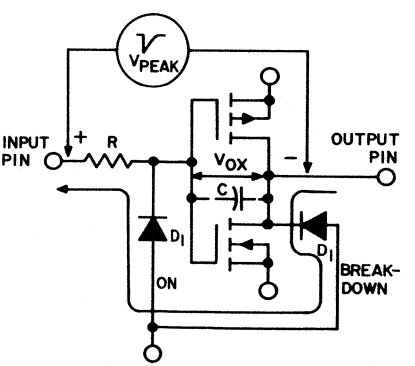
$V_{OXIDE\ MAX} = V_{DI\ ON} = 1$ V
n-TYPE UNIT

(d)



$V_{OXIDE\ MAX} = V_{OXIDE\ MAX} = VD_I$ (BREAKDOWN) + VD_I (ON) = 25 V + 1 V = 26 V
n-TYPE UNIT p-TYPE UNIT

(e)



$V_{OXIDE\ MAX} = V_{OXIDE\ MAX} = VD_I$ (ON) + VD_I (BREAKDOWN)
= 1 V + 25 V = 26 V
n-TYPE UNIT p-TYPE UNIT

(f)

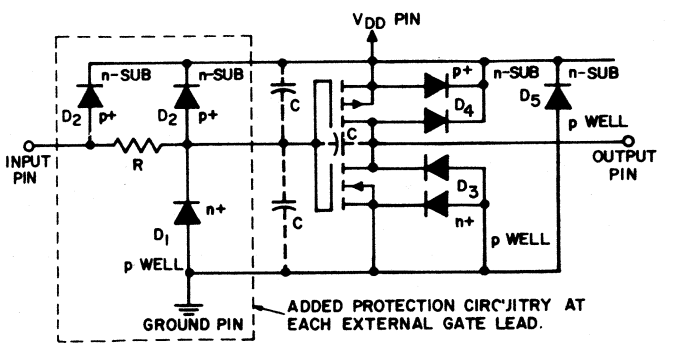
Fig. 40 — Input circuits designed to limit extraneous voltages to safe levels under all operating conditions.

The breakdown voltage of an MOS gate oxide is in the order of 100 volts; the dc resistance in the order of 10^{12} ohms. In contrast to semiconductor diodes in which the breakdown limit can be tested any number of times without damaging the device, the MOS gate oxide is shorted as a result of only one voltage excursion to the breakdown limit. Because of the extremely high resistance of the gate oxide, even a very-low-energy source (such as a static charge) is capable of developing this breakdown voltage.

The input resistance R, as shown in Fig. 39, is nominally between 1 and 3 kilohms. This value, in conjunction with the capacitances of the gate and the associated protective diodes, integrates and clamps the device voltages to a safe level. Fig. 40 demonstrates how input circuits can be designed to limit extraneous voltages to safe levels under all operating conditions. Because of the low RC time constants of these circuits, they have no noticeable effect on circuit speed and do not interfere with logic operation.

In circuits that contain gate-protection circuits, the power-supply voltage V_{DD} should not be turned off while a signal from a low-impedance pulse generator is applied at any of the inputs to the COS/MOS IC. The reason for this restriction can be understood with the aid of Fig. 40(a) where the V_{DD} line is essentially grounded so that a positive voltage input from a pulse generator is impressed across diodes D_2. This voltage, of between 3 and 15 volts, could cause permanent damage to the doides or could burn out the V_{DD} metallization. Therefore, if, in any system design, any input excursion is expected to exceed $+V_{DD}$ or fall below $-V_{SS}$, the current through the input doides should be limited to 50 milliamperes to assure safe operation.

Fig. 41 shows the over-all protection circuit (interconnected



DIODE BREAKDOWNS

D_1 = n^+ TO p WELL 25 V MAX

D_2 = p^+ TO n SUB 50 V

D_3 = n SUB TO p WELL 100 V

R = NORMAL p^+ DIFFUSION IN n SUB ISOLATION

Fig. 41 – Gate-oxide protection circuit used in COS/MOS integrated circuits.

with a COS/MOS inverter) that is incorporated into all RCA COS/MOS integrated circuits. In addition to the basic input protection discussed in the preceding paragraphs, all inverter outputs and all transmission-gate inputs and outputs are fully protected by substrate diodes (D3, D4, and D5), as shown in Fig. 41.

Features and Characteristics of RCA COS/MOS Integrated Circuits (CD4000A Series)

The RCA family of COS/MOS digital integrated circuits includes a standard line of devices (the CD4000A series) designed to operate from voltage supplies of 3 to 15 volts. Each pellet in the series is supplied in both ceramic and plastic packages so that all devices included in the series are available in two different operating temperature ranges. Devices supplied in the ceramic flat-pack (CD4000AK-series), dual-in-line ceramic (CD4000AD-series), and TO-5-style (CD4000AT-series) packages operate over the temperature range of -55°C to +125°C. Devices supplied in the dual-in-line plastic (CD4000AE-series) packages operate over a temperature range of -40°C to +85°C. The storage-temperature range for all packages is from -65°C to +150°C. Table I lists the **maximum ratings** for the RCA

Table I – Maximum Ratings (Absolute Maximum Values)

	CD4000AK,AD,AT	CD4000AE
Recommended Operating Voltage Range (V_{DD}-V_{SS}) (Volts)	3 to 15	
DC Supply Voltage (Volts)	-0.5 to +15	
Dissipation per package (milliwatts)	200	
Operating Temperature Range (°C)	-55 to +125	-40 to +85
All Inputs*	$V_{SS} \leq V_{IN} \leq V_{DD}$	
Storage Temperature Range (°C)	-65 to +150	

*For types CD4009A and CD4010A, $V_{SS} \leq V_{CC} \leq V_{DD}$

CD4000A series of COS/MOS digital integrated circuits.

The ratings shown in Table I are based on the **Absolute Maximum System** and are limiting values of operating and environmental conditions that should not be exceeded by any circuit of a specified type under any conditions of operation. Effective use of these ratings requires close control of supply-voltage variations, component variations, equipment-control adjustment, load variations, and environmental conditions.

FUNCTIONAL CLASSIFICATIONS AND LOGIC DIAGRAMS

The RCA CD4000A series of COS/MOS integrated circuits provides the equipment designer with a very comprehensive line of circuits for a wide variety of logic-system applications. This series of circuits includes arithmetic devices, counter/dividers, decoders, flip-flops, gates, hex-buffers, multiplexers, shift registers, and latches. These circuits feature low power requirements, wide operating voltage range, high noise immunity, fully protected inputs, excellent temperature stability, and high fanout capabilities. Table II lists COS/MOS circuits currently included in the CD4000A series and indicates the logic function for which each circuit is normally used. Figs. 42 through 50 show the logic diagrams for circuits included in the CD4000A series.

Table II – RCA CD4000A-Series COS/MOS Integrated Circuits

Gates	
CD4000A	Dual 3-Input NOR Gate Plus Inverter
CD4001A	Quad 2-Input NOR Gate
CD4002A	Dual 4-Input NOR Gate
CD4011A	Quad 2-Input NAND Gate
CD4012A	Dual 4-Input NAND Gate
CD4019A	Quad AND-OR Select Gate
CD4023A	Triple 3-Input NAND Gate
CD4025A	Triple 3-Input NOR Gate
CD4030A	Quad Exclusive–OR Gate
CD4037A	Triple AND-OR Bi-Phase Pairs
Flip-Flops	
CD4013A	Dual "D" with Set/Reset Capability
CD4027A	Dual J-K with Set/Reset Capability
Latches	
CD4042A	Quad Clocked "D" Latch
CD4043A	NOR R/S Latch (3 Output States)
CD4044A	NAND R/S Latch (3 Output States)

Table II – RCA CD4000A-Series COS/MOS Integrated Circuits – cont'd

Arithmetic Devices

CD4008A	Four-Bit Full Adder, Parallel Carry-Out
CD4032A	Triple Serial Adder, Internal Carry (Neg. Logic)
CD4038A	Triple Serial Adder, Internal Carry (Pos. Logic)

Buffers

CD4009A	Hex Inverting Type
CD4010A	Hex Non-Inverting Type
CD4041A	Quad Inverting and Non-Inverting Type

Complementary Pairs

CD4007A	Dual Complementary Pair Plus Inverter

Multiplexers and Decoders

CD4016A	Quad Bilateral Switch
CD4028A	BCD-to-Decimal Decoder

Counters

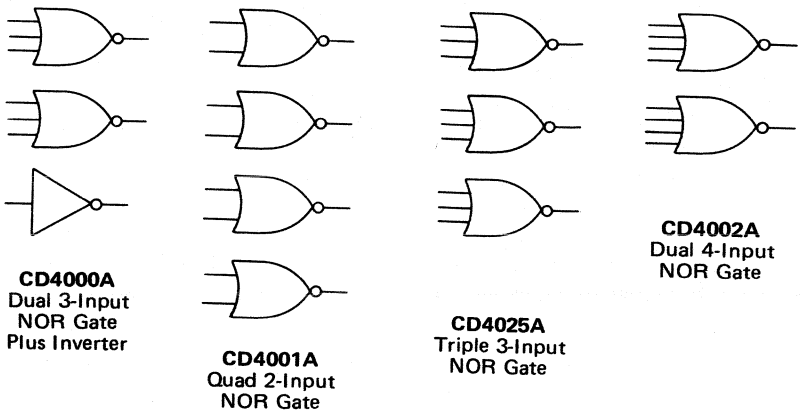
CD4017A	Decoded Counter/Divider Plus 10 Decoded Dec. Outputs
CD4018A	Presettable Divide-by-N Counter
CD4020A	14-Stage Ripple Counter
CD4022A	Divide-by-N Counter/Divider, 8 Decoded Outputs
CD4024A	7-Stage Ripple Counter
CD4026A	Decade Counter/Divider, 7-Segment Display Output
CD4029A	Presettable Up/Down Counter, Binary or BCD-Decade
CD4033A	Decade Counter/Divider, 7-Segment Display Output
CD4045A	21-Stage Ripple Counter

Shift Registers

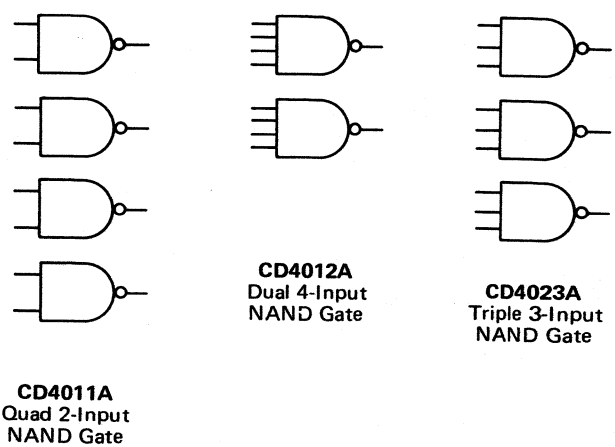
CD4006A	18-Stage Static Shift Register
CD4014A	8-Stage Synch Shift Register Parallel-In/Serial Out
CD4015A	Dual 4-Stage Shift Register, Serial-In/Parallel-Out
CD4021A	8-Stage Asynchronous Shift Register, Parallel-In/Serial-Out
CD4031A	64-Stage Static Shift Register
CD4034A	Parallel-In, Parallel-Out Shift Register (3 Output States)
CD4035A	4-Bit Parallel-In, Parallel-Out Shift Register, J-$\overline{K}$ In, True-Comp. Out
CD4036A	Quad 8-Bit Storage Register (Binary Addressing)
CD4039A	Quad 8-Bit Storage Register (4-Line Addressing)

Phase-Locked Loop

CD4046A	Micropower Phase-Locked Loop

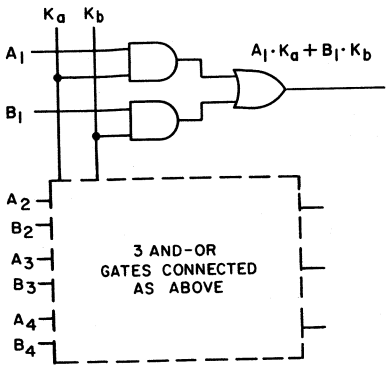


(a) NOR gates

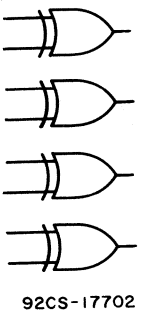


(b) NAND gates

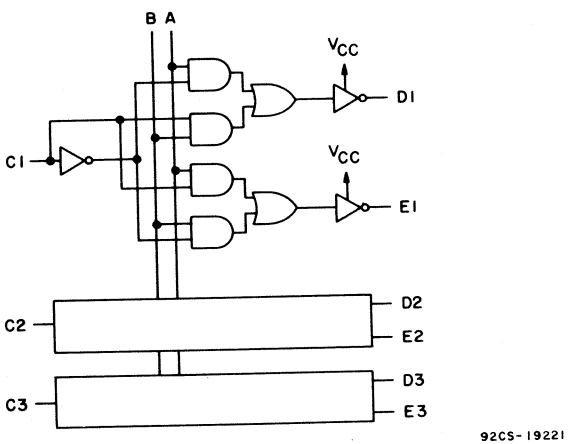
Fig. 42 – Logic diagrams for COS/MOS gate circuits
(continued on page 38).



CD4019A
Quad AND-OR
Select Gate



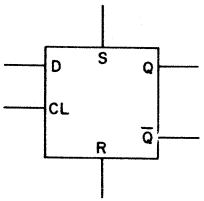
CD4030A
Quad
Exclusive-OR
Gate

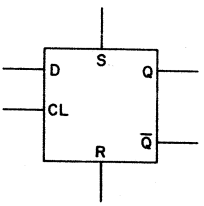


CD4037A
Triple AND-OR
Bi-Phase
Pairs

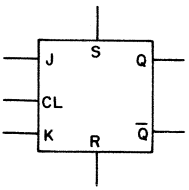
(c) Gate arrays

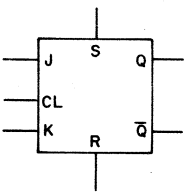
Fig. 42 – Logic diagrams for COS/MOS gate circuits (continued from page 37).



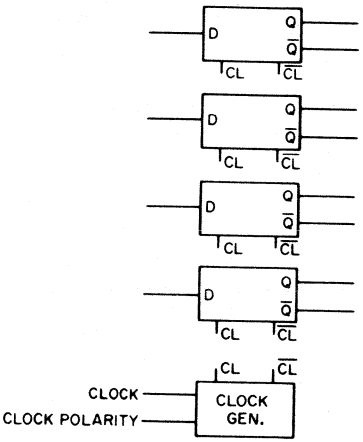


CD4013A
Dual "D" Flip-Flop with Set/Reset Capability

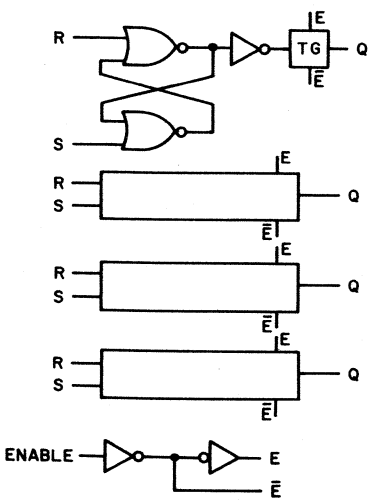




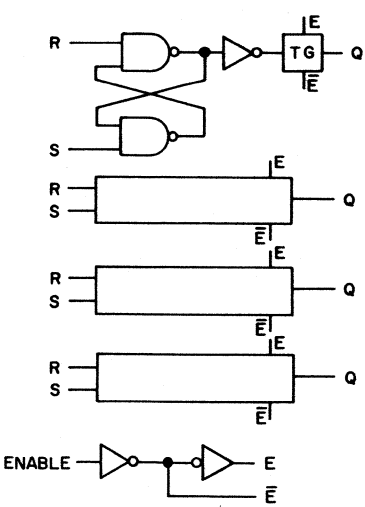
CD4027A
Dual J-K Flip-Flop with Set/Reset Capability



CD4042A
Quad Clocked "D" Latch

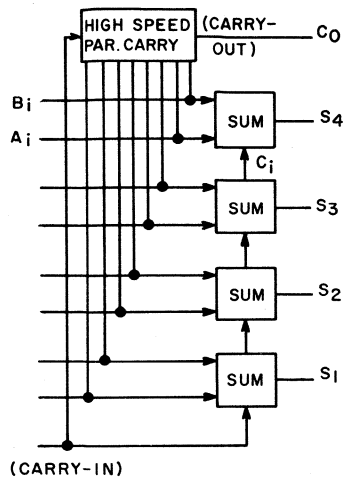


CD4043A
Quad NOR R/S Latch
(3 Output States)

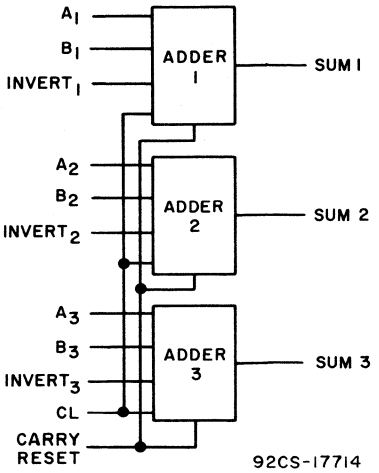


CD4044A
Quad NAND R/S Latch
(3 Output States)

Fig. 43 — Logic diagrams for COS/MOS flip-flops and latches.

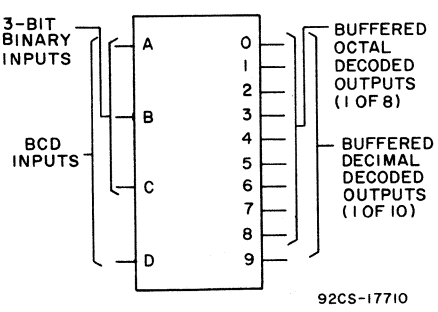


CD4008A
Four Bit
Full Adder with
Parallel Carry Out

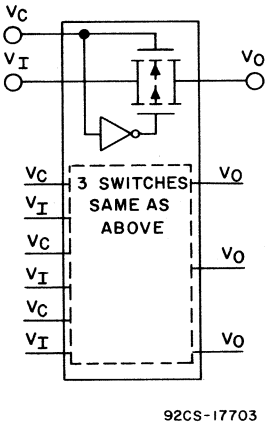


CD4032A, CD4038A
Triple Serial Adders with Internal Carry
CD4032A—Negative-Logic Adder
CD4038A—Positive-Logic Adder

Fig. 44 — Logic diagrams for COS/MOS arithmetic devices.

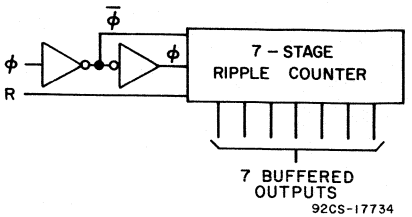


CD4028A
BCD-to-Decimal
Decoder

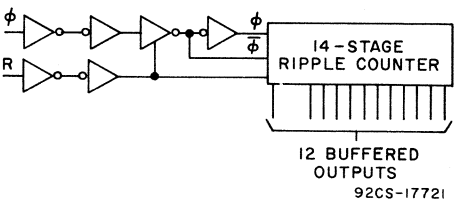


CD4016A
Quad Bilateral Switch

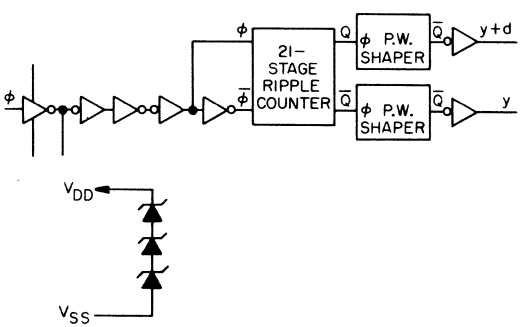
Fig. 45 — Logic diagrams for COS/MOS decoders and multiplexers.



CD4024A
7-Stage
Binary Counter
with Buffered Reset



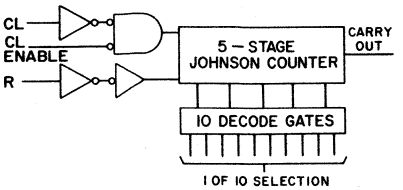
CD4020A
14-Stage
Ripple-Carry
Binary Counter/Divider



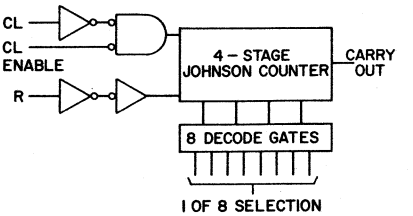
CD4045A
21-Stage
Ripple-Carry

(a) Ripple-carry types

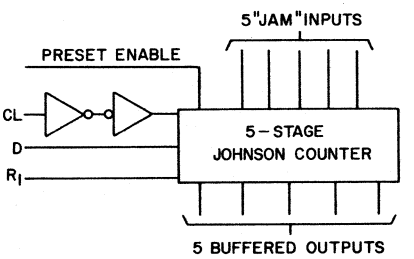
Fig. 46 – Logic diagrams for COS/MOS counters (continued on pages 42 and 43).



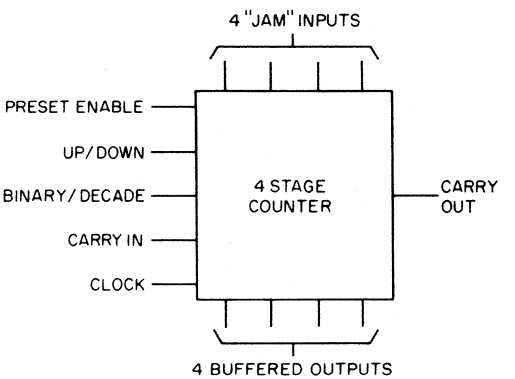
CD4017A
Decade Counter/
Divider Plus 10
Decoded Decimal Outputs



CD4022A
Divide-by-8
Counter/Divider
with 8 Decoded Outputs



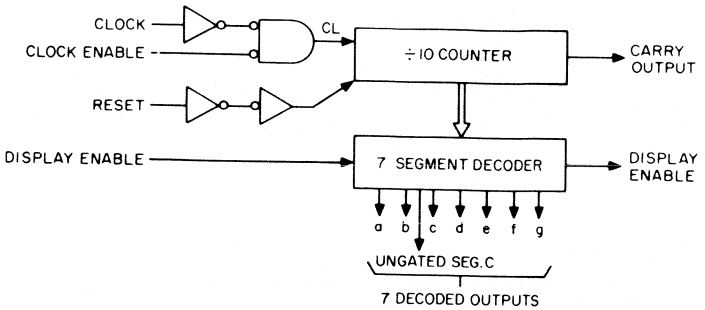
CD4018A
Presettable, Divide-by-"N" Counter
Fixed or Programmable
Divide by 2 through 10



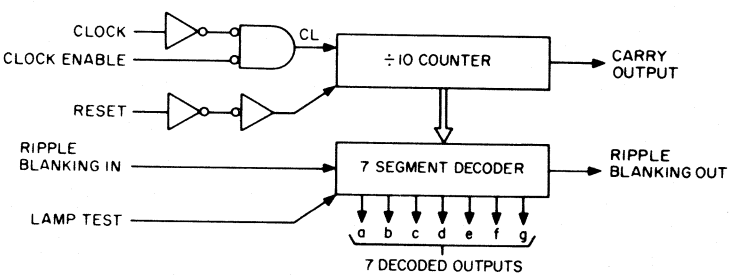
CD4029A
Presettable, Up/Down Counter,
Binary or BCD-
Decade

(b) Synchronous types

Fig. 46 – Logic diagrams for COS/MOS counters
(continued on page 43).



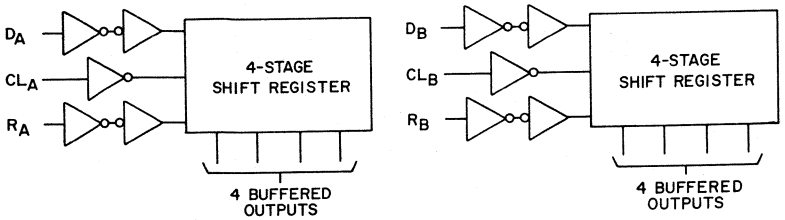
CD4026A
Decade Counter/Divider with
7-Segment Display Outputs and
Display Enable



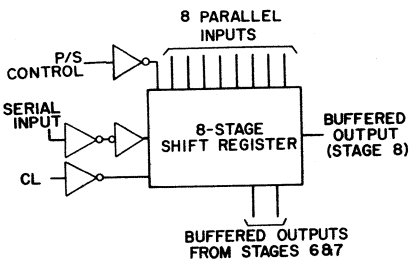
CD4033A
Decade Counter/Divider With
7-Segment Display Outputs
and Ripple Blanking

(c) Decade with 7-segment decoder types

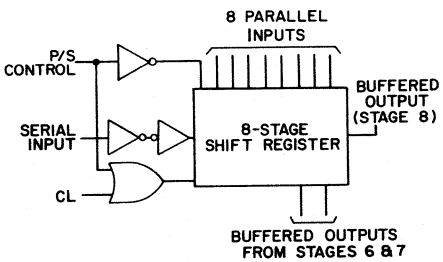
Fig. 46 – Logic diagrams for COS/MOS counters (continued from pages 41 and 42).



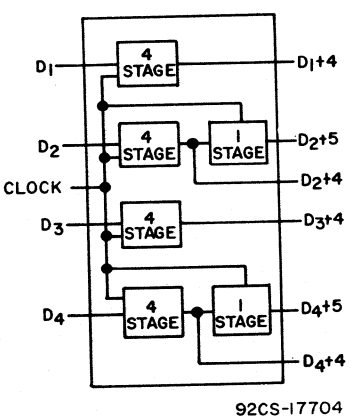
CD4015A
Dual 4-Stage
with Serial Input/
Parallel Output



CD4014A
8-Stage Synch.
Parallel Input/
Serial Output



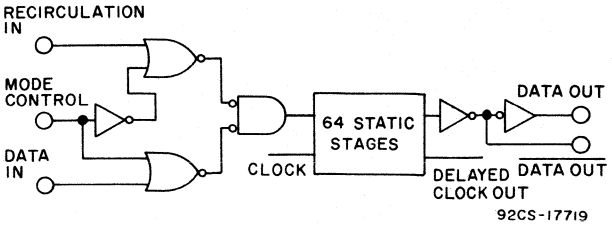
CD4021A
8-Stage Asynch.
Parallel Input/
Serial Output



CD4006A
18-Stage

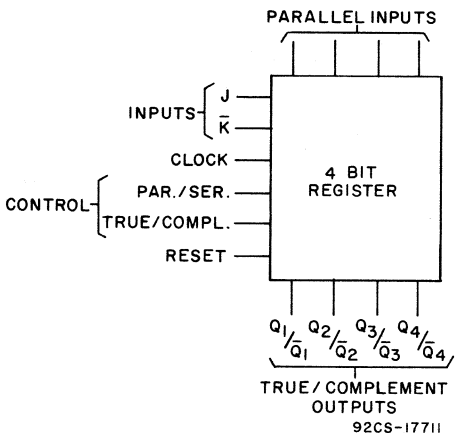
(a) Static shift registers

Fig. 47 — Logic diagrams for COS/MOS shift registers
(continued on page 45).

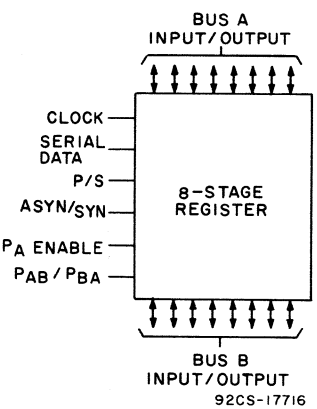


CD4031A
64-Stage

(a) Static shift registers (cont'd)



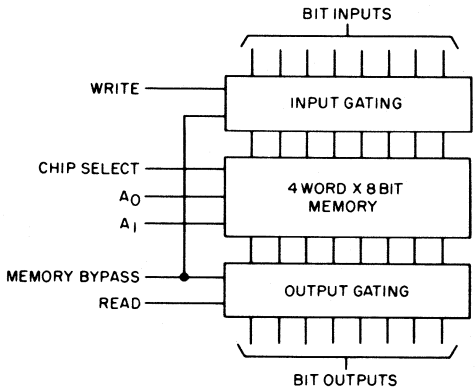
CD4035A
4-Bit with J-$\overline{K}$ Input and
True/Complement Output



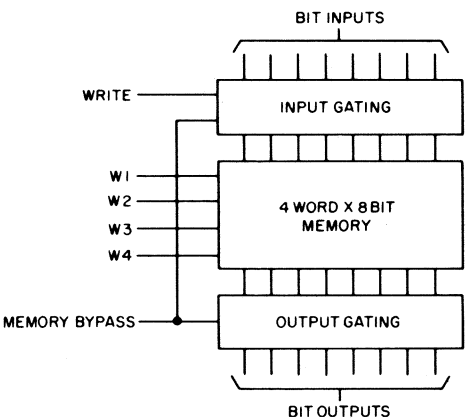
CD4034A
8-Stage Static Bidirectional
Parallel/Serial Input/Output
Bus Register
(3 Output States)

(b) Parallel-in/parallel-out shift registers

Fig. 47 — Logic diagrams for COS/MOS shift registers
(continued from page 44).

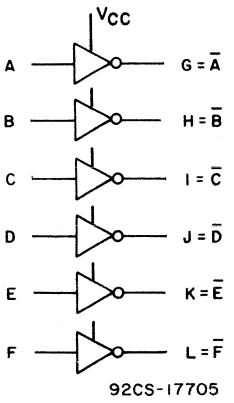


CD4036A
Quad 8-Bit Storage Register
(Binary Addressing)

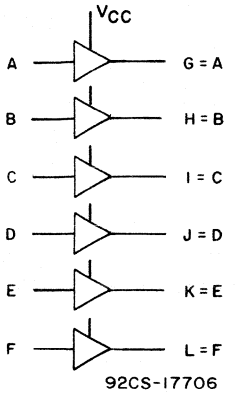


CD4039A
Quad 8-Bit Storage Register
(4-Line Addressing)

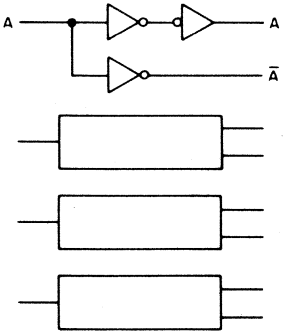
Fig. 48 – Logic diagrams for COS/MOS storage registers (memories).



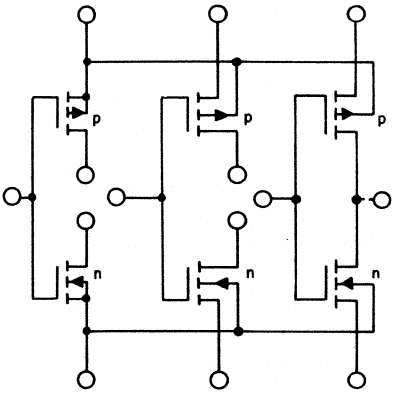
CD4009A
Hex Inverting Type



CD4010A
Hex Non-Inverting Type



CD4041A
Quad Inverting and
Non-Inverting Type



CD4007A
Dual Complementary
Pair Plus Inverter

Fig. 49 — Logic diagrams for COS/MOS Buffers.

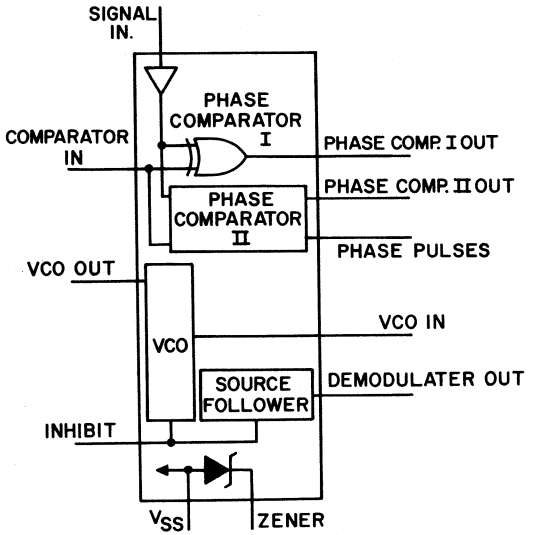


Fig. 50 – Logic diagram for COS/MOS phase-locked loop.

PERFORMANCE CHARACTERISTICS

The CD4000A families of logic and MSI devices offer many unique performance characteristics not found in other IC technologies. The following paragraphs contain tables and graphs of important performance parameters. Complete information concerning any device can be found in the appropriate data sheet. For the utilization and applicability of these performance characteristics, reference should be made to the sections in this Manual concerning **COS/MOS Logic-System Design** and **Applications.**

Quiescent Power Dissipation

Table III illustrates the extremely low quiescent (dc) power consumption of the COS/MOS family. Static or standby power is normally in the microwatt region. The **quiescent power dissipation** shown is per package with supply voltages, V_{DD}, of 5 and 10 volts; V_{SS} is 0 volts; and T_A is 25°C. Both typical and maximum dissipation values are given.

Output Drive Current

COS/MOS devices will normally drive inputs to other COS/MOS

Table III — Quiescent Power Dissipation (P_D) Per Package (All values in μW except as noted)

Series Types	Typical				Limits (max)			
	Series 4000AK,AD		Series 4000AE		Series 4000AK,AD		Series 4000AE	
	V_{DD} = 10V	5V	10V	5V	10V	5V	10V	5V
Gates								
NOR CD4000A,01A,02A,25A	0.01	0.005	0.05	0.025	1	0.25	10	2.5
NAND CD4011A,12A,23A	0.01	0.005	0.05	0.025	1	0.25	10	2.5
Dual Complementary Pair Plus Inverter CD4007A	0.01	0.005	0.05	0.025	1	0.25	10	2.5
Multiplexer (Bilaterial Switch) CD4016A	0.1	–	0.1	–	5	–	5	–
AND/OR Select CD4019A	0.5	0.15	2	0.5	100	25	1000	250
Exclusive-OR CD4030A	0.1	0.025	1	0.25	10	2.5	100	25
Buffers								
Inverting CD4009A	0.1	0.05	0.5	0.15	5	1.5	50	15
Non-Inverting CD4010A	0.1	0.05	0.5	0.15	5	1.5	50	15
True/Complement CD4041A	0.05	0.025	0.2	0.05	20	5	200	50
Triple AND/OR Bi-Phase Pairs CD4037A	0.5	0.15	2	0.5	100	25	1000	250
Flip-Flops								
Dual "D" CD4013A	0.05	0.025	0.2	0.05	20	5	200	50
Dual J-K CD4027A	0.5	0.025	0.2	0.05	20	5	200	50
Latches								
Clocked "D" CD4042A	0.05	0.025	0.2	0.05	10	5	200	50
NOR R/S CD4043A	0.05	0.025	0.2	0.05	20	5	200	50
NAND R/S CD4044A	0.05	0.025	0.2	0.05	20	5	200	50
Counters and Registers								
7-Stage Binary Counter CD4024A	5	1.5	10	2.5	100	25	1000	250
14-Stage Binary Counter CD4020A	10	2.5	20	5	250	75	1000	250
18-Stage Static Shift Register CD4006A	0.1	0.05	0.5	0.15	10	2.5	100	25

Table III – Quiescent Power Dissipation (P_D) Per Package (All values in μW except as noted) – cont'd

Series Types	Typical				Limits (max)			
	Series 4000AK,AD		Series 4000AE		Series 4000AK,AD		Series 4000AE	
	V_{DD} = 10V	5V	10V	5V	10V	5V	10V	5V
Counters and Registers cont'd								
1/N Counter CD4018A	5	1.5	10	2.5	100	25	1000	250
1/8 Counter CD4022A	5	1.5	10	2.5	100	25	1000	250
Decade Counters CD4017A,26A,33A	5	1.5	10	2.5	100	25	1000	250
Up/Down Counter CD4029A	5	1.5	10	2.5	100	25	1000	250
21-Stage Counter CD4045A	15	3.75	30	7.5	–	–	–	–
8-Stage Static Registers CD4014A,21A	10	2.5	10	2.5	100	25	1000	250
Dual 4-Stage Static Register CD4015A	10	2.5	10	2.5	100	25	1000	250
64-Stage Static Shift Register CD4031A	10	2.5	20	5	250	50	1000	250
MSI 8-Stage Static Register CD4034A	5	1.5	–	–	100	25	–	–
4-Stage Register CD4035A	5	1.5	10	2.5	100	25	1000	250
Arithmetic								
Full 4-Bit Adder CD4008A	5	1.5	10	2.5	100	25	1000	250
Serial Adders CD4032A,38A	5	1.5	10	2.5	100	25	1000	250
Decoder								
BCD-to-Decimal CD4028A	10	2.5	100	2.5	100	25	1000	250
Memories								
4-word-by-8-Bit NDRO CD4036A,39A	5	1.5	–	–	–	–	–	–

devices; these other devices appear as purely capacitive loads. Therefore, except during switching, no output **source** or **sink current** flows. In some instances, however, COS/MOS devices are directly interfaced with other logic forms. Table IV provides typical and maximum output sink and source currents for COS/MOS devices.

Noise Immunity

The noise-immunity data shown in Table V are expressed in terms of absolute values referenced above or below the normal-state level for which the logic level will change state. For example, if the device input is at a logic 1 level of +10 volts (V_{DD} of 10 volts) and the guaran-

Table IV – Output Drive Current [$I_D(p)$ (–); $I_D(n)$ (+)] (All values in mA)

Series Types	Typical				Limits (min)							
	Series 4000A				Series 4000AK,AD				Series 4000AE			
	V_{DD} = 10V		5V		10V		5V		10V		5V	
	$I_D(p)$	$I_D(n)$	$I_D(p)$	$I_D(n)$	$I_D(p)$	$I_D(n)$	$I_D(p)$	$I_D(n)$	$I_D(p)$	$I_D(n)$	$I_D(p)$	$I_D(n)$
Gates												
NOR												
CD4000A,01A,02A,25A	-1	2.5	-2[a]	1	-0.5	0.9	-0.5[a]	0.4	-0.25	0.6	-0.3[a]	0.3
NAND												
CD4011A,23A	-1.2	0.6	-0.5	0.5	-0.6	0.5	-0.25	0.25	-0.3	0.25	-0.12	0.12
CD4012A	-1.2	0.6	-0.5	0.25	-0.6	0.25	-0.25	0.12	-0.3	0.13	-0.12	0.6
Dual Complementary Pair Plus Inverter												
CD4007A	-2.5	2.5	-4.0	1	-1.1	1.3	-1.4[a]	0.6	-0.55	1.0	-1.1[a]	0.3
AND/OR Select												
CD4019A	-1.5	2.5	-0.5	1.5	-0.7	1.2	-0.25	0.7	-0.5	0.75	-0.12	0.35
Exclusive-OR												
CD4030A	-1.3	2.4	-0.6	1.2	-0.65	0.6	-0.23	0.6	-0.32	0.6	-0.15	0.3
Buffers												
Inverting												
CD4009A	-0.8	10	-1.75[a]	4	-0.6	8	-1.25[a]	3	-0.6	8	-1.25[a]	3
Non-Inverting												
CD4010A	-0.8	10	-1.75[a]	4	-0.6	8	-1.25[a]	3	-0.6	8	-1.25[a]	3
Triple AND/OR Bi-Phase Pairs												
CD4037A	-2.5	2.5	-1	1	–	–	–	–	–	–	–	–
True/Complement												
CD4041A												
True Output	-8	10	-2.8	3.2	-4	5	-1.4	1.6	-2	2.5	-0.7	0.8
Comp. Output	-3.6	4	-1.2	1.6	-1.8	2	-0.6	0.8	-0.9	1	-0.3	0.4
Flip-Flops												
Dual "D"												
CD4013A	-1.3	2.5	-0.5	1	-0.65	1	-0.25	0.5	-0.33	0.6	-0.14	0.3
Dual J-K												
CD4027A	-1.3	2.5	-0.5	1	-0.65	1	-0.25	0.5	-0.33	0.6	-0.14	0.3
Latches												
Clocked "D"												
CD4042A	-2	2	-1	1	-0.9	1	-0.35	0.4	-0.45	0.5	-0.175	0.2
NOR R/S												
CD4043A	-1	1	-0.5	0.5	-0.4	0.5	-0.175	0.2	-0.2	0.25	-0.009	0.1
NAND R/S												
CD4044A	-1	1	-0.5	0.5	-0.4	0.5	-1.75	0.2	-0.2	0.25	-0.009	0.1
Counters and Registers												
7-Stage Binary Counter												
CD4024A	-0.7	1	-0.3	0.5	-0.35	0.5	-0.15	0.25	-0.25	0.25	-0.12	0.12
14-Stage Binary Counter												
CD4020A	-0.5	0.6	-0.25	0.4	-0.20	0.3	-0.09	0.15	-0.15	0.15	-0.6	0.08
18-Stage Static Shift Register												
CD4006A	-0.3	0.5	-0.15	0.25	-0.2	0.25	-0.1	0.125	-0.1	0.125	-0.05	0.06

Table IV – Output Drive Current [$I_D(p)$ (–); $I_D(n)$ (+)] (All values in mA) – cont'd

Series Types	Typical				Limits (min)							
	Series 4000A				Series 4000AK,AD				Series 4000AE			
	V_{DD} = 10V		5V		10V		5V		10V		5V	
	$I_D(p)$	$I_D(n)$	$I_D(p)$	$I_D(n)$	$I_D(p)$	$I_D(n)$	$I_D(p)$	$I_D(n)$	$I_D(p)$	$I_D(n)$	$I_D(p)$	$I_D(n)$
Counters and Registers (cont'd)												
64-Stage Static Shift Register												
CD4031A												
Q Output	-1.4	8	-0.64	2.6	-0.7	–	-0.32	1.3	-0.35	–	-0.16	1.3
$\overline{Q}$ Output	-0.4	0.4	-0.18	0.18	-0.2	0.2	-0.09	0.09	-0.1	0.1	-0.045	0.045
CL_D Output	-1.6	2.4	-0.8	0.8	-0.8	1.2	-0.4	0.4	-0.4	0.6	-0.2	0.6
MSI 8-Stage Static Register												
CD4034A	-0.25	0.5	-0.1	0.2	-0.125	0.25	-0.05	0.1	–	–	–	–
1/N Counter												
CD4018A												
Q5 Output	-1	1	-0.4	0.4	-0.35	0.35	-0.15	0.15	-0.25	0.25	-0.08	0.08
Other Outputs	-0.4	0.4	-0.15	0.1	-0.2	0.2	-0.06	0.05	-0.15	0.15	-0.03	0.025
1/8 Counter												
CD4022A												
Decode	-0.15	0.3	-0.075	0.15	-0.15	0.1	-0.03	0.05	-0.05	0.05	-0.015	0.025
Carry	-0.8	1	-0.4	0.5	-0.3	0.3	-0.15	0.15	-0.13	0.13	-0.08	0.08
Decade Counters												
CD4017A												
Decode	-0.2	0.4	-0.075	0.1	-0.1	0.1	-0.03	0.05	-0.07	0.07	-0.015	0.025
Carry	-1	1	-0.4	0.4	-0.35	0.35	-0.15	0.15	-0.24	0.25	-0.08	0.08
CD4026,33A												
Decode	-0.6	0.5	-0.28	0.24	-0.3	0.25	-0.14	0.12	-0.15	0.12	-0.07	0.06
Carry	-1	1	-0.4	0.4	-0.35	0.35	-0.15	0.15	-0.24	0.25	-0.08	0.08
21-Stage Counter												
CD4045A	-6	6	-2.5	2.5	–	–	–	–	–	–	–	–
Up/Down Counter												
CD4029A												
Q Output	-0.4	1.2	-0.24	0.8	-0.2	0.6	-0.12	0.4	-0.1	0.3	-0.06	0.2
Carry	-0.2	0.64	-0.12	0.16	-0.1	0.32	-0.06	0.08	-0.05	0.16	-0.03	0.04
8-Stage Static Registers												
CD4014A,21A	-0.44	0.5	-0.16	0.3	-0.2	0.25	-0.08	0.12	-0.1	0.1	-0.05	0.06
Dual 4-Stage Register												
CD4015A	-0.44	0.5	-0.16	0.3	-0.2	0.25	-0.08	0.12	-0.1	0.1	-0.05	0.06
Arithmetic												
Full 4-Bit Adder												
CD4008A												
Carry	-1.5	1.5	-0.5	0.5	-0.75	0.75	-0.25	0.25	-0.5	0.5	-0.13	0.13
Sum[b]	-0.3	0.5	-0.02	0.02	-0.15	0.25	-0.01	0.01	-0.1	0.2	-0.007	0.007
Serial Adders												
CD4032A,38A	-1.2	2.4	-0.4	0.09	-0.55	0.7	-0.15	0.5	-0.27	0.5	-0.1	0.2
Decoder												
BCD-to-Decimal												
CD4028A	-1.9	2.4	-0.9	1.2	-0.95	1.2	-0.45	0.6	-0.48	0.6	-0.22	0.3

[a] Output voltage V_O = 2.5V

[b] V_O (sum) = 3 V

Table V – Noise Immunity
($V_{NIH} = -V_{NIL}$ unless otherwise specified; all values in volts)

Series Types	Typical		Limits	
	V_{DD} = 10V	5V	10V	5V
All except as noted	±4.5	±2.25	±3	±1.5
Inverting Buffer, CD4009A	±4.5	±2.25	V_{NIL} = 2 V_{NIH} = -3	V_{NIL} = 1 V_{NIH} = -1.5

teed noise immunity for the device is 3 volts, the device will not change state when the input level drops from +10 to 7 volts because of noise. Similarly, if the input is at 0 volts (logic 0) under the same conditions, the device will not change state when noise signals of 3 volts appear at the input. The interfering or noise voltage may be of either a slow drift variety (dc), transient in nature (ac), or a combination of both.

Unit-Load Characteristics

A **unit load** is defined for COS/MOS devices as the load represented by any single input terminal of a gate-level device. Because every COS/MOS input terminal is connected to a pair of insulated gates via a standard gate-oxide protection circuit, the unit load is purely capacitive. The typical unit load is 5 picofarads including the package. Table VI lists the number of unit loads represented by each signal input terminal.

Speed and propagation delay data are given in subsequent tables as a function of the number of unit loads.

Table VI – Unit Load Characteristics (C_I)
(All values in pF)

Series Types	Typical		
	Inputs	V_{DD} = 10V	5V
All except as noted	All	5	5
AND/OR Select CD4019A	a,b	5	5
	k_a,k_b	12	12
4-Bit Full Adder CD4008A	All	10	10
18-Stage Static Shift Register CD4006A	Clock	30	30
	Data	5	5

Propagation Delay and Clock Frequency

Table VII shows the **propagation delay** limits for all COS/MOS devices. Both tpHL and tpLH propagation

Table VII — Propagation Delay (tpHL, tpLH) — Output Load Capacitance C_L = 15 pF (All values in ns)

Series Types	Typical				Limits (max)							
	Series 4000A				Series 4000AK,AD				Series 4000AE			
	V_{DD} = 10V		5V		10V		5V		10V		5V	
	HL	LH	HL	LH	HL	LH	HL	LH	HL	LH	HL	LH
Gates												
NOR CD4000A,01A, 02A,25A	25	25	35	35	40	45	50	95	55	65	80	120
NAND CD4011A,23A,	25	25	50	50	40	40	75	75	50	50	100	100
CD4012A	50	25	100	50	75	40	150	75	100	50	200	100
Dual Complementary Pair Plus Inverter CD4007A	20	20	35	35	40	40	60	60	50	50	75	75
Multiplexer CD4016A												
Turn On	20	20	NOT AVAILABLE									
Signal In to Signal Out	10	10	NOT AVAILABLE									
AND/OR Select CD4019A	50	50	100	100	100	100	225	225	125	125	300	300
Exclusive-OR CD4030A	40	40	100	100	100	100	200	200	150	150	300	300
Triple AND-OR Bi-Phase Pairs CD4037A	75	75	225	225	150	150	450	450	200	200	650	650
Buffers												
Inverting CD4009A	10	25	15	50	30	55	55	80	40	70	70	100
Non-Inverting CD4010A	10	25	15	50	30	55	55	80	40	70	70	100
True/Complement CD4041A												
True Output	40	45	65	75	75	75	115	125	100	100	140	150
Comp. Output	30	25	55	45	45	40	100	100	65	60	125	125
Flip-Flops												
Dual "D" CD4013A	75	75	150	150	110	110	300	300	125	125	350	350
Dual J-K CD4027A	75	75	150	150	110	110	300	300	150	150	400	400
Latches												
Quad Clocked "D" CD4042A	75	75	150	150	125	125	300	300	200	200	400	400
Quad NOR R/S CD4043A	75	75	175	175	175	175	350	350	200	200	400	400
Quad NAND R/S CD4044A	75	75	175	175	175	175	350	350	200	200	400	400
Counters and Registers												
7-Stage Binary Counter CD4024A	80	80	175	175	125	125	350	350	150	150	400	400
14-Stage Binary Counter CD4020A	150	150	450	450	225	225	600	600	250	250	650	650

Table VII — Propagation Delay (tpHL, tpLH) — Output Load Capacitance C_L = 15 pF (All values in ns) — cont'd

Series Types	Typical				Limits (max)							
	Series 4000A				Series 4000AK,AD				Series 4000AE			
	V_{DD} = 10V		5V		10V		5V		10V		5V	
	HL	LH	HL	LH	HL	LH	HL	LH	HL	LH	HL	LH
Counters and Registers (cont'd)												
18-Stage Static Shift Register												
CD4006A	125	125	250	250	200	200	400	400	250	250	500	500
1/N Counter												
CD4018A												
$\overline{Q}_5$ Output	125	125	350	350	250	250	1000	1000	300	300	1300	1300
Other Outputs	200	200	500	500	400	400	1200	1200	500	500	1600	1600
1/8 Counter												
CD4022A												
Carry	125	125	325	325	250	250	1000	1000	500	500	1300	1300
Decode	200	200	400	400	400	400	1200	1200	800	800	1600	1600
Decade Counter												
CD4017A												
Carry	125	125	350	350	250	250	1000	1000	300	300	1300	1300
Decode	200	200	500	500	400	400	1200	1200	500	500	1600	1600
Up/Down Counter												
CD4029A												
Q Outputs	115	115	325	325	230	230	650	650	460	460	1300	1300
Carry	150	150	425	425	300	300	850	850	600	600	1700	1700
8-Stage Static Registers												
CD4014A,21A	100	100	300	300	225	225	750	750	300	300	1000	1000
Dual 4-Stage Static Register												
CD4015A	100	100	300	300	225	225	750	750	300	300	1000	1000
64-Stage Static Shift Register												
CD4031A	200	200	400	400	400	400	800	800	800	800	1600	1600
MSI 8-Stage Static Register												
CD4034A	240	240	600	600	480	480	1200	1200	–	–	–	–
4-Stage Shift Register												
CD4035A	100	100	250	250	200	200	500	500	700	700	300	300
Arithmetic												
Full-Bit Adder												
CD4008A												
At Output												
From Sum Input	325	325	900	900	500	500	1300	1300	650	650	2000	2000
From carry input	325	325	900	900	500	500	1300	1300	650	650	2000	2000
At Carry Output												
From sum input	120	120	320	320	200	200	600	600	240	240	800	800
From carry input	45	45	100	100	75	75	175	175	90	90	200	200
Serial Adders												
CD4032A,38A												
At Sum Output												
From A,B, or invert. inputs	125	125	400	400	250	250	1100	1100	300	300	1400	1400
From clock input	250	250	800	800	500	500	2200	2200	600	600	2400	2400
Decoder												
BCD-to-Decimal												
CD4028A	100	100	250	250	180	180	480	480	290	290	700	700

delays are shown. For all sequential circuits, such as flip-flops, counters, or registers, delay is from clock input to Q or $\overline{Q}$ outputs. Table VII gives delays for 3 unit loads; i.e., for a COS/MOS device driving three COS/MOS unit-load inputs. Propagation delays for unit loads ranging from 1 to 20 and for supply voltages of 5, 10, and 15 volts are shown in the curves of Fig. 51.

Table VIII shows typical maximum clock frequencies **(toggle rates)** for all sequential devices; the data in Table VIII are given for 3 unit loads. Table IX shows maximum clock rise and fall times. Fig. 52 shows maximum input clock frequency as a function of supply voltage at 3 unit loads.

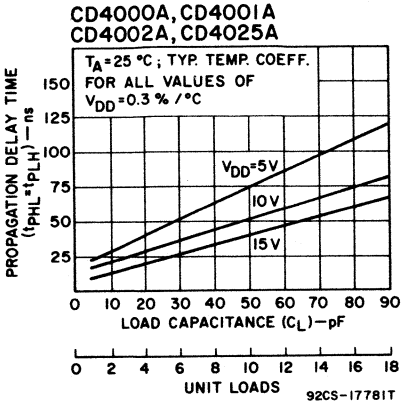
Table VIII – Sequential Devices Maximum Input Clock Frequency (Toggle Rate), f(max)–Output Load Capacitance C_L = 15 pF (All values in MHz)

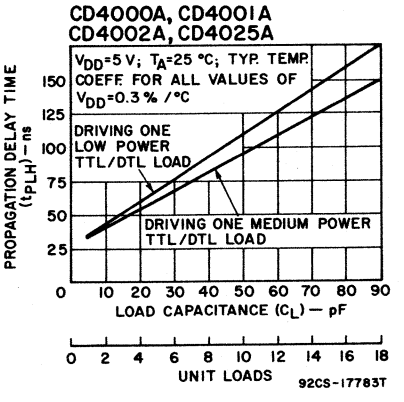
Series Types	Typical Series 4000A V_{DD} = 10V	Typical Series 4000A 5V	Limits (min) Series 4000AK,AD 10V	Limits (min) Series 4000AK,AD 5V	Limits (min) Series 4000AE 10V	Limits (min) Series 4000AE 5V
Flip-Flops						
Dual "D" CD4013A	10	4	7	3	5	2.5
Dual J-K CD4027A	8	3	4.5	1.5	3	1
Counters and Registers						
7-Stage Binary Counter CD4024A	7	2.5	4	1.5	3	1
14-Stage Binary Counter CD4020A	7	2.5	4	1.5	3	1
4-Stage Shift Register CD4035A	5	2.5	3	1.5	2	1
MSI 8-Stage Static Register CD4034A	5	2.5	3	1.5	–	–

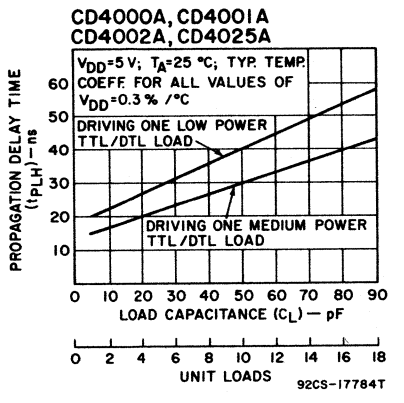
Table VIII — Sequential Devices Maximum Input Clock Frequency (Toggle Rate) f(max)—Output Load Capacitance C_L = 15 pF (All values in MHz) — cont'd

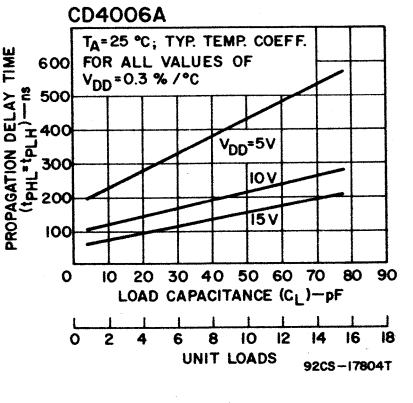
Series Types	Typical Series 4000A		Limits (min) Series 4000AK,AD		Series 4000AE	
	V_{DD} = 10V	5V	10V	5V	10V	5V
18-Stage Static Shift Register CD4006A	5	2.5	2.5	1	2	0.6
64-Stage Static Shift Register CD4031A	4	2	2	0.8	1	0.4
1/N Counter CD4018A	5	2.5	3	1	2	0.6
1/8 Counter CD4022A	5	2.5	3	1	2	0.6
Decade Counters						
CD4017A	5	2.5	3	1	2	0.6
CD4026A, 33A	5	2.5	3	1.5	2	1
Up/Down Counter CD4029A	5	2.5	3	1.5	2	1
8-Stage Static Registers CD4014A,21A	5	2.5	3	1	2.5	0.6
Dual-Stage Static Register CD4015A	5	2.5	3	1	2.5	0.6
Quad Bilateral Switch CD4016A	10*					

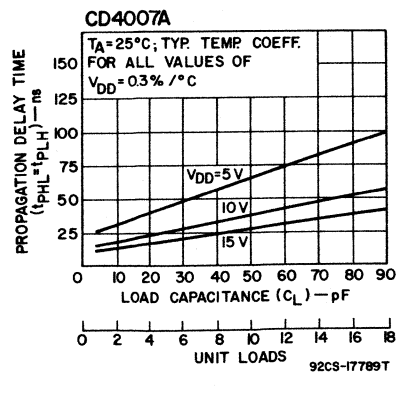
*Control Input Repetition Rate











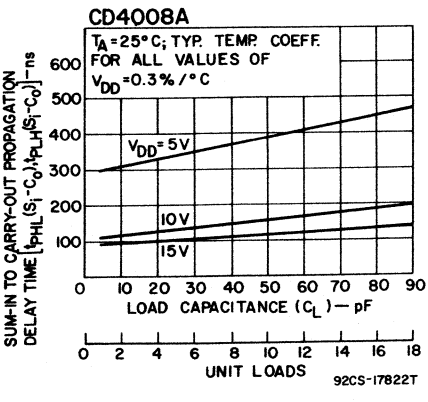
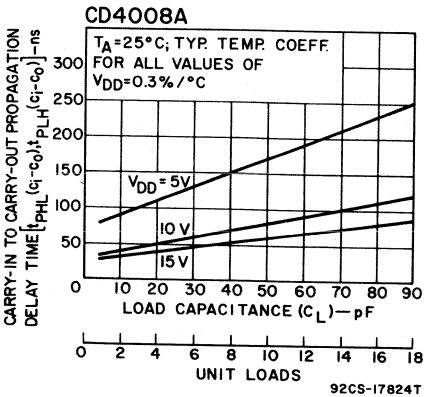
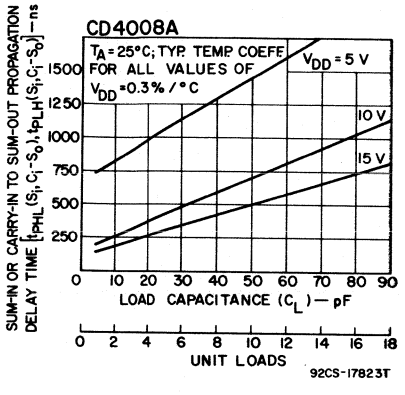
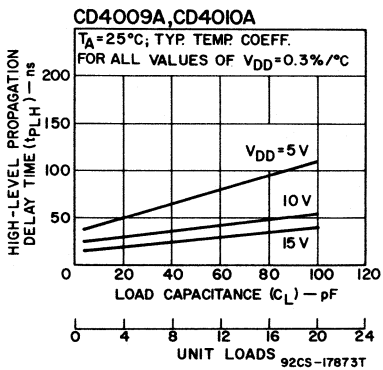
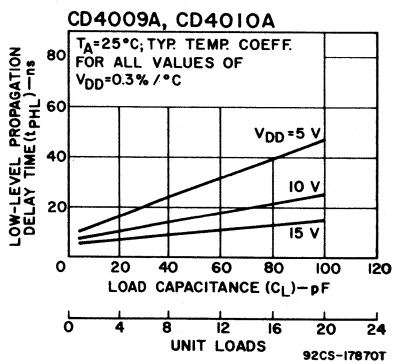


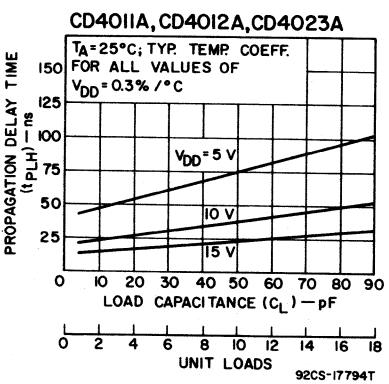
Fig. 51 — Propagation delay as a function of load capacitance and number of unit loads for CD4000A-series devices; curves apply equally to all device types in a series. (sheet 1 of 6)











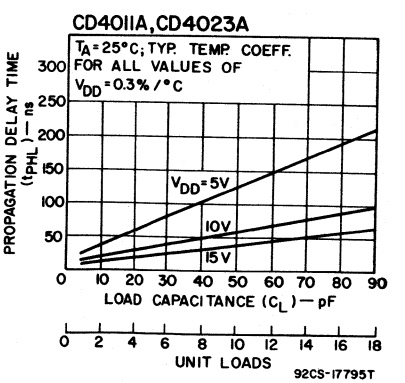
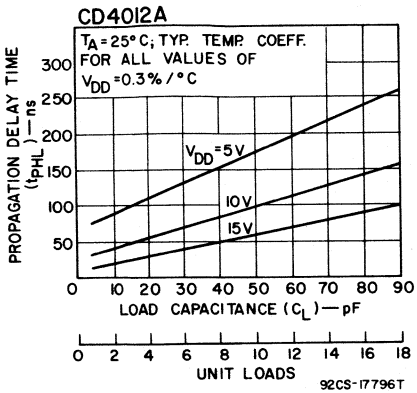
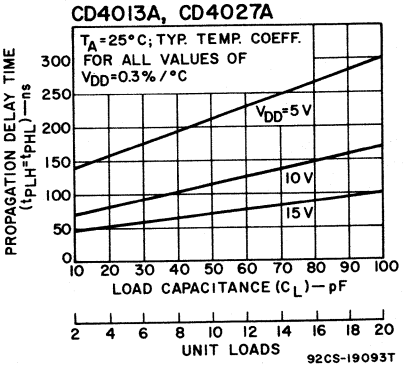
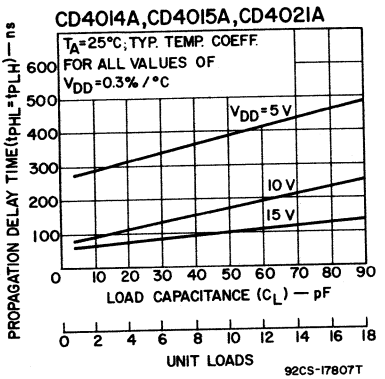
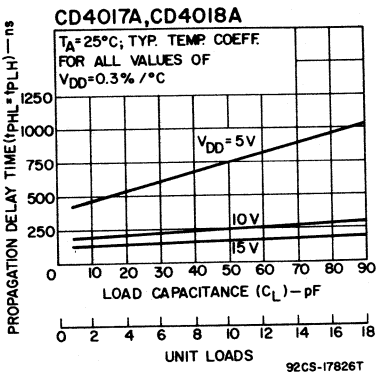


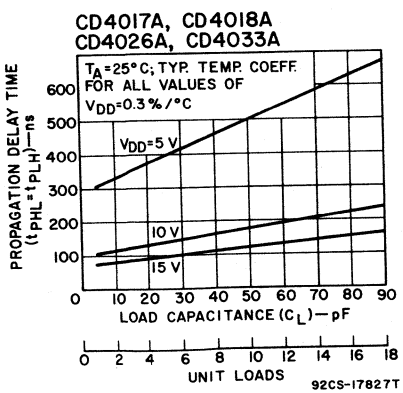
Fig. 51 — Propagation delay as a function of load capacitance and number of unit loads for CD4000A-series devices; curves apply equally to all device types in a series. (sheet 2 of 6)











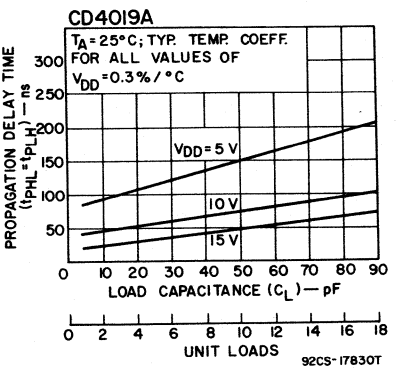


Fig. 51 — Propagation delay as a function of load capacitance and number of unit loads for CD4000A-series devices; curves apply equally to all device types in a series. (sheet 3 of 6)

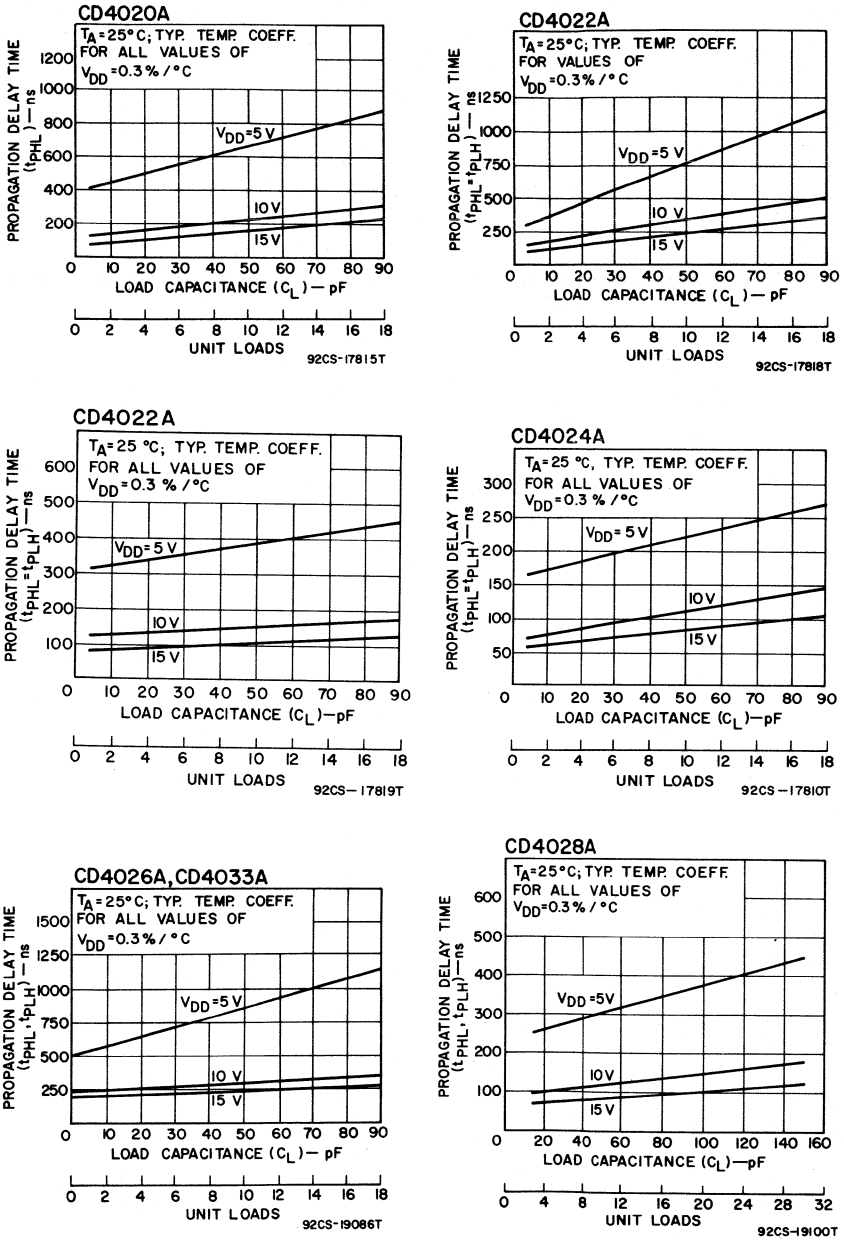
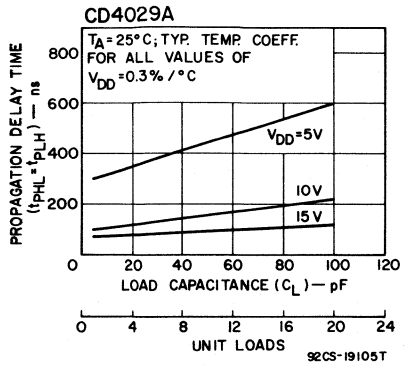
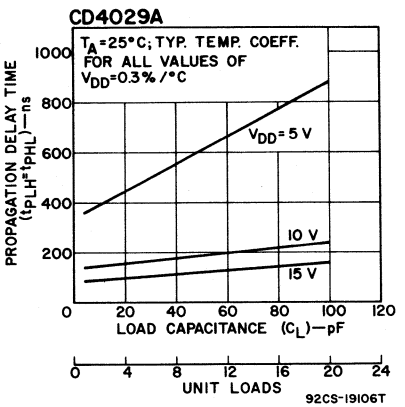
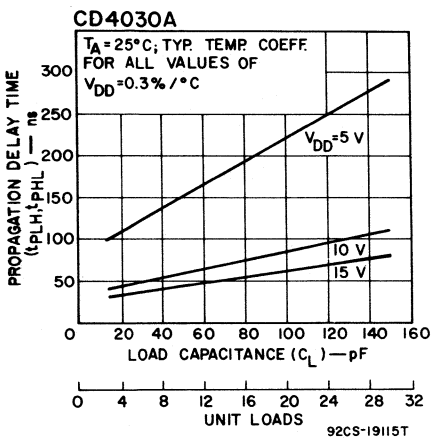
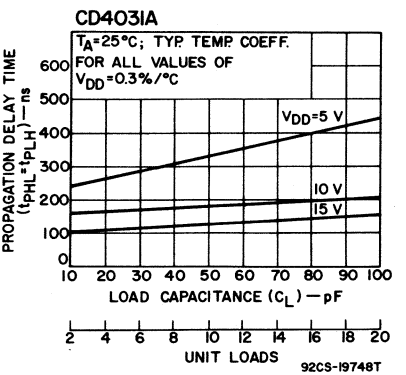


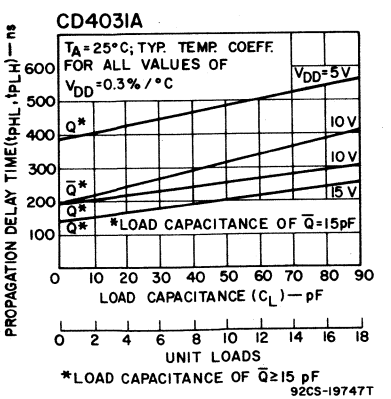
Fig. 51 — Propagation delay as a function of load capacitance and number of unit loads for CD4000A-series devices; curves apply equally to all device types in a series. (sheet 4 of 6)











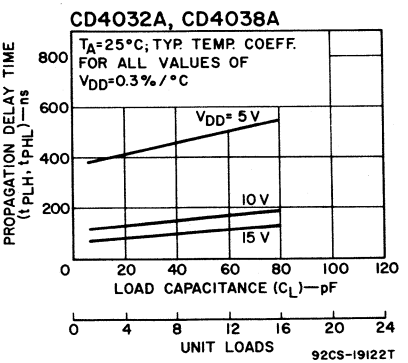


Fig. 51 — Propagation delay as a function of load capacitance and number of unit loads for CD4000A-series devices; curves apply equally to all device types in a series. (sheet 5 of 6)

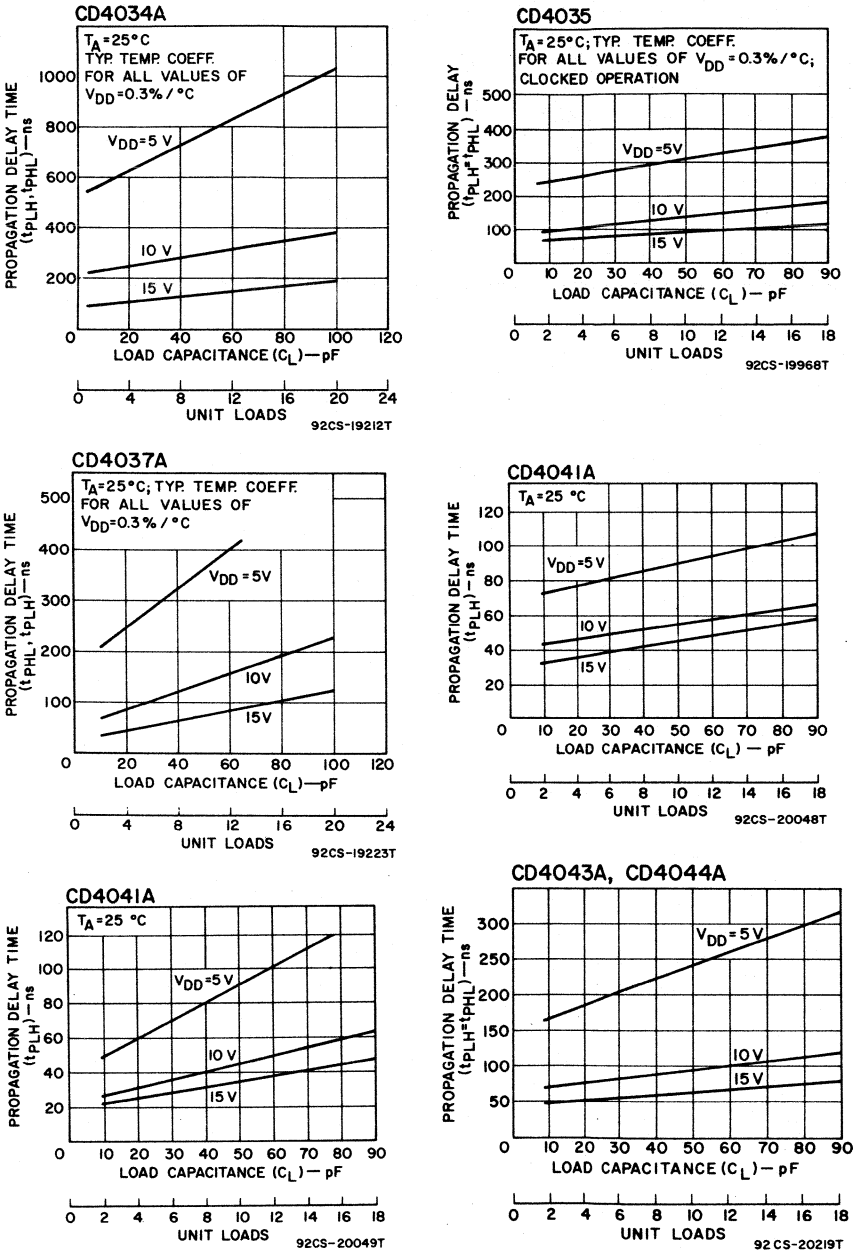
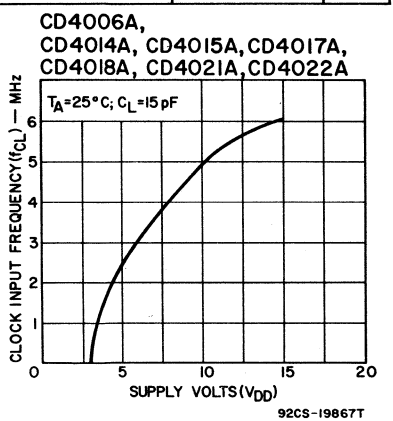
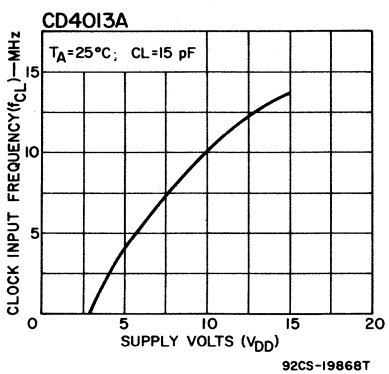


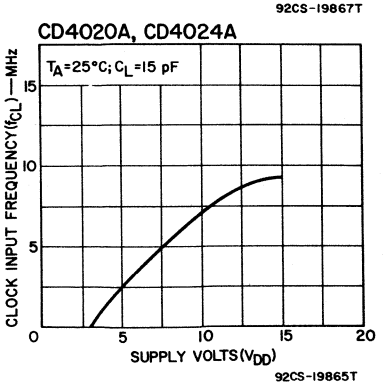
Fig. 51 — Propagation delay as a function of load capacitance and number of unit loads for CD4000A-series devices; curves apply equally to all devices of a series (sheet 6 of 6).

Table IX – Maximum Clock Rise and Fall Times, $t_r(CL) = t_f(CL)$
(All values in microseconds)

Series Types	Limits (max.) Series 4000AK, AD V_{DD} = 10V	5V
All Except as Noted	15	15
Dual "D" Flip-Flops CD4013A	5	15
7-Stage Binary Counter CD4024A	10	15
64-Stage Static Shift Register CD4031A	1	2
4-Stage Shift Register CD4035A	5	15
Latches CD4042A CD4043A CD4044A	5	15







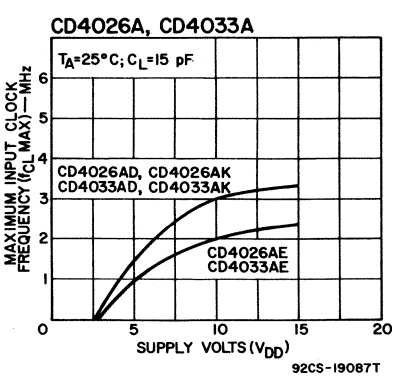
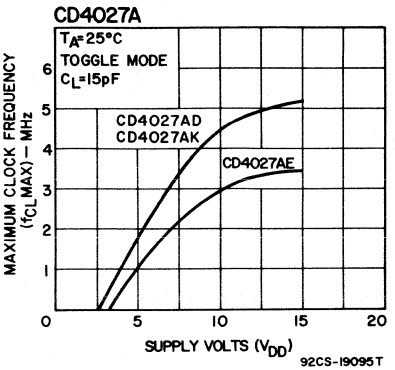
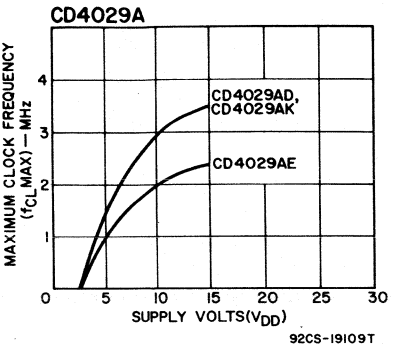
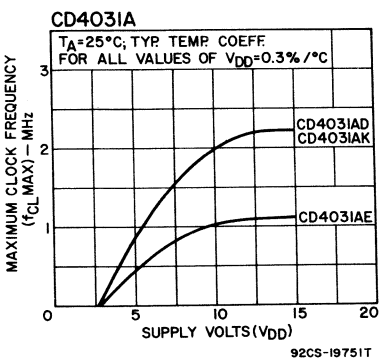
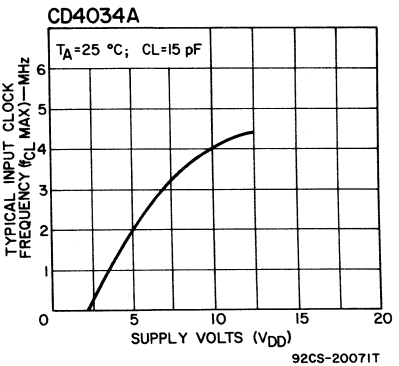


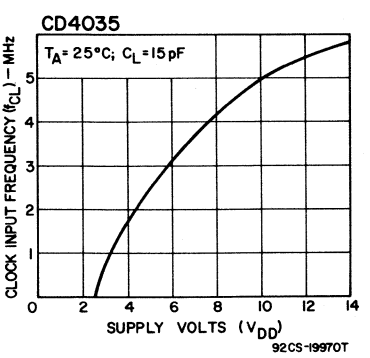
Fig. 52 – Maximum input clock frequency (toggle rate) as a function of supply voltage for CD4000A-series devices; curves apply equally to all device types in a series. (sheet 1 of 2)











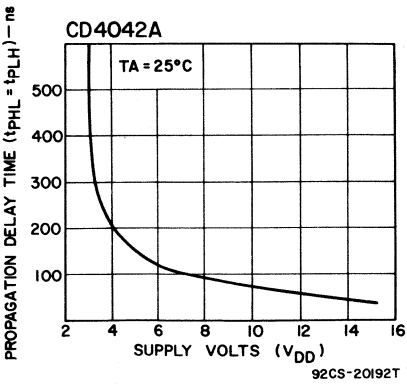
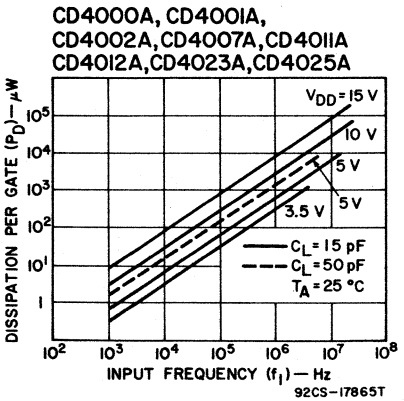
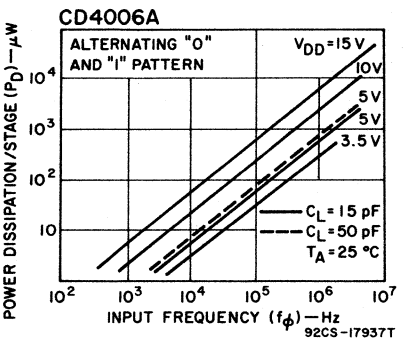


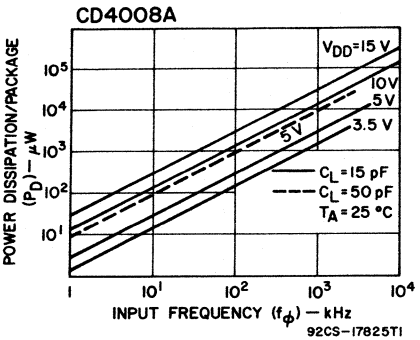
Fig. 52 — Maximum input clock frequency (toggle rate) as a function of supply voltage for CD4000A-series devices; curves apply equally to all device types in a series. (sheet 2 of 2)

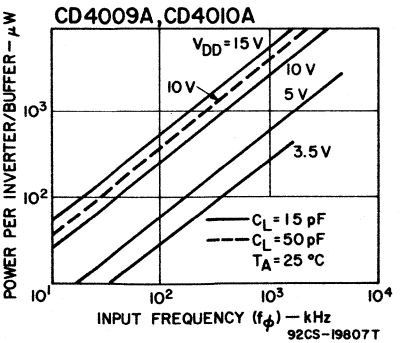
Typical Dynamic Power Consumption

Power dissipation in COS/MOS devices is a function of load capacitance (ac fan-out), supply voltage, and switching frequency. A family of power-dissipation versus frequency curves is given in Fig. 53. Curves are shown for a fan-out of 3 unit loads and supply voltages of 3.5, 5, 10, and 15 volts.









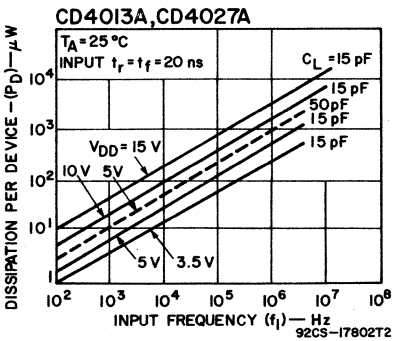
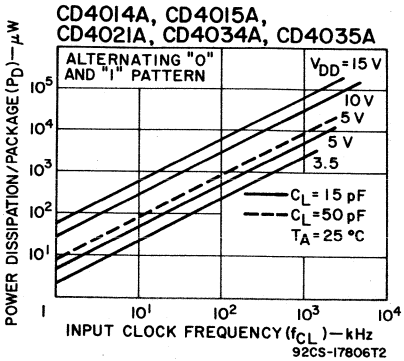
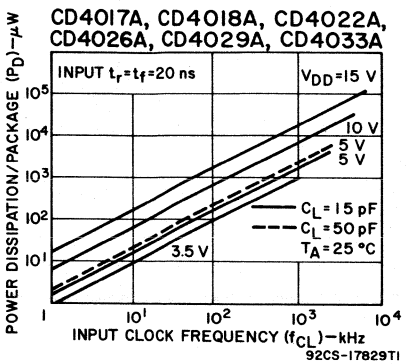
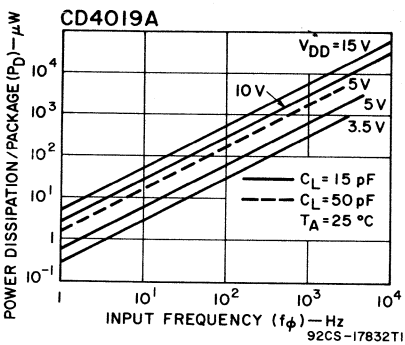
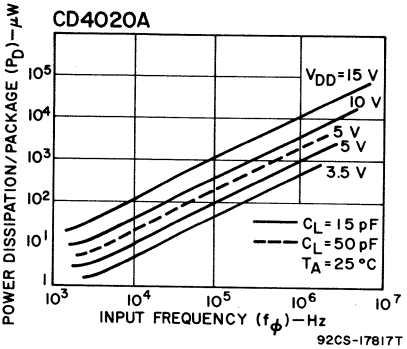


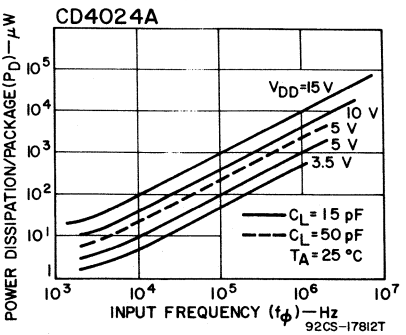
Fig. 53 — Power dissipation as a function of frequency for CD4000A-series devices; curves apply equally to all device types in a series. (sheet 1 of 3)











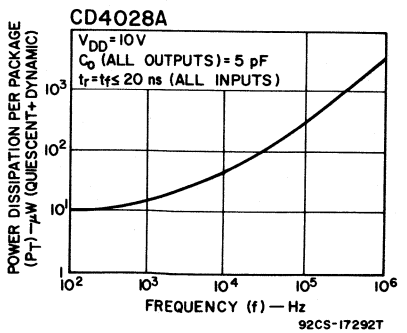
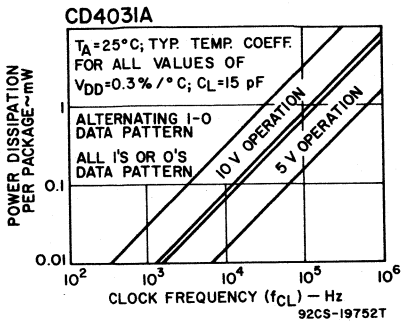
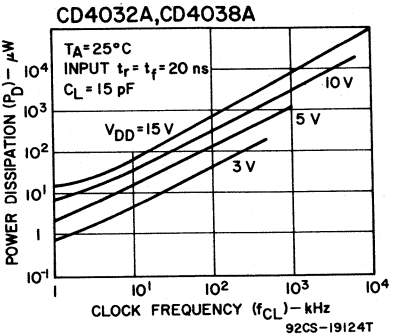
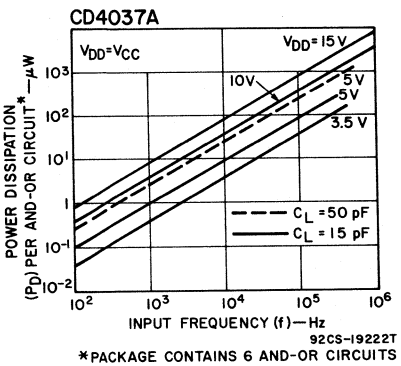
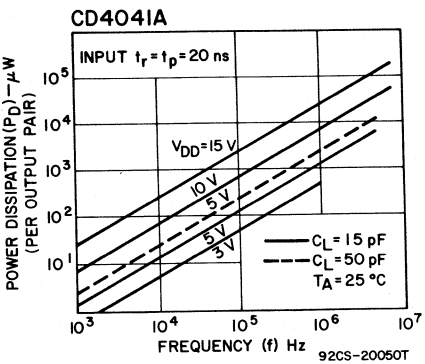


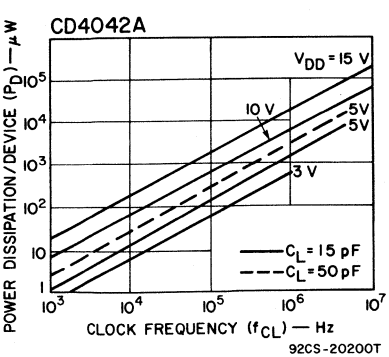
Fig. 53 — Power dissipation as a function of frequency for CD4000A-series devices; curves apply equally to all device types in a series. (sheet 2 of 3)











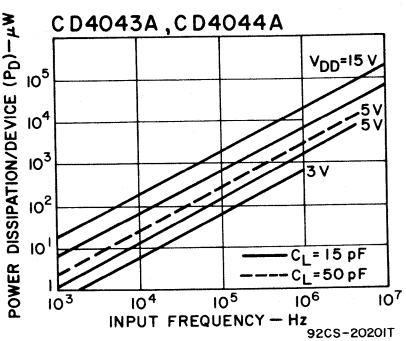


Fig. 53 – Power dissipation as a function of frequency for CD4000A-series devices; curves apply equally to all device types in a series. (sheet 3 of 3)

COS/MOS Logic-System Design Rules

Successful and efficient logic design using the CD4000A series of COS/MOS integrated circuits can be achieved by following the guidelines described in this section. Handling of unused inputs, power-supply polarity and range considerations, and logic busing are all discussed. As an aid to COS/MOS logic-system design, special attention is given to the topics of system power calculation, noise immunity, interfacing with other logic forms, and power-source and filtering requirements.

MAXIMUM-RATING CONSIDERATIONS

The first rule in the design of a COS/MOS logic system is to make certain that no maximum rating of a COS/MOS integrated circuit will be exceeded under any condition of operation. The power-supply voltage should never be applied to a COS/MOS integrated circuit in the reverse polarity. Application of a reverse voltage greater than 0.5 volt may damage the integrated circuit. Input signals should not exceed the power-supply range unless special precautions are taken to limit current through the input protective diodes. The V_{CC} terminal of the CD4009A and CD4010A circuits must never be more positive than the V_{DD} voltage, although this terminal can be connected to the same voltage value if these circuits are to be used as non-level-shifting buffers.

SHORT-CIRCUIT CONSIDERATIONS

In most cases, COS/MOS outputs can be accidentally shorted to either V_{DD} or V_{SS} without damage to the device because the normal saturation region of the drain-source characteristic limits the short-circuit current. However, very-high-current devices that operate at high voltage, such as the CD4009A, CD4010A, or CD4041A, can easily dissipate more than 200 milliwatts under short-circuit conditions, as shown in Fig. 54. Shorted outputs can cause ex-

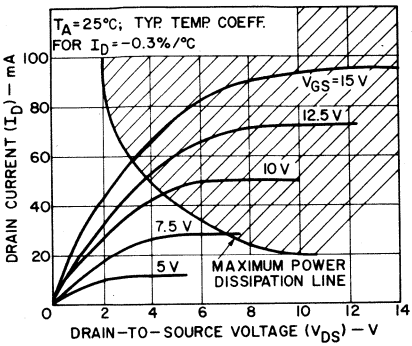


Fig. 54 – Maximum dissipation of one CD4009A or CD4010A COS/MOS integrated circuit.

cessive dissipation, as can direct drive of the bases of bipolar power transistors.

UNUSED INPUTS

In a COS/MOS device, all input terminals must be connected to a voltage level between V_{SS} (the most negative potential) and V_{DD} (the most positive potential). In circuit configurations in which input terminals connect directly to NAND gates, the **unused inputs** must be tied to V_{DD} (high-level state) or tied together with another input terminal to a signal source. Either of these connections is necessary because the output of any NAND gate normally remains in the high-level state for as long as any input is in a low-level state; the output changes to a low-level state only when all inputs are high.

Conversely, in circuits which connect directly to NOR gates, the unused inputs must be tied to V_{SS} (low-level state, usually ground) or connected together to another input terminal driven by a signal source. Either of these connections is required because the output of a NOR gate is in the low-level state if any input is in the high-level state. The output of the NOR gate goes high only when all inputs are low.

Floating inputs, (unused inputs) guarantee neither a logic 0 nor a logic 1 condition at the output of the device, but cause increased susceptibility to circuit noise and can result in excessive power dissipation. Floating inputs to high-impedance COS/MOS gates can result in linear-region noise biasing when both the p- and n-type devices are ON.

INPUT SIGNAL SWING

For optimum performance results, high-level logic inputs should be made equal to V_{DD}, and low-level logic inputs should be made equal to V_{SS}. COS/MOS data sheets indicate that a logic 1 output is $V_{DD} - 0.01$ volts (positive logic) and a logic 0 output is 0.01 volt. However, because of the high dc noise immunity of COS/MOS, an acceptable logic 1 is $V_{DD} - 0.7\ V_{DD}$, and an acceptable logic 0 is $V_{SS} + 0.3\ V_{SS}$. Fig. 55 shows the range of switching transfer characteristics for a COS/MOS integrated circuit for a supply voltage V_{DD} of 10 volts.

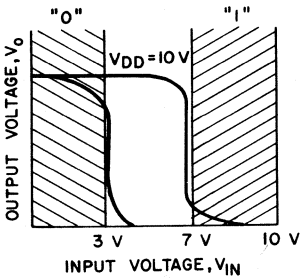


Fig. 55 – Range of switching transfer characteristics.

PARALLELING GATE INPUTS

The inputs of multi-input NAND and NOR gates are sometimes wired together and connected to a common source. In the case of NAND gates, where as many as 4 input pins may be wired together (CD4012A), a slight increase in speed occurs when more than one input is tied to the same signal, as shown in Fig. 56. More importantly, however, the output source current of the device is increased proportionately to the number of inputs wired together.

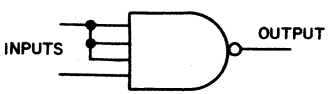


Fig. 56 — Logic diagram of 4-input NAND gate with 3 inputs interconnected.

When the inputs of a NOR gate are tied together in a common input signal, the gate experiences a higher sink current and a slight increase in speed. The speed increase in both NAND and NOR gates results from the lower ON resistance of the paralleled devices. The increase in speed is minimized by a compensating speed decrease caused by the added capacitance of the driving source as well as capacitance internal to the device itself.

PARALLEL INPUTS AND OUTPUTS OF GATES AND INVERTERS

Both source and sink output current are increased when two or more similar devices on the same chip are paralleled as shown in Fig. 57. This increased drive capability also increases speed if the increase in capacitive loading is not excessive. When devices are paralleled, power dissipation also increases.

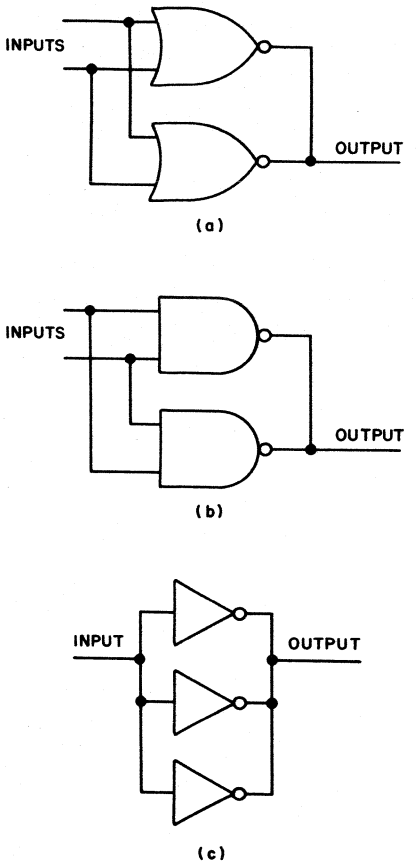


Fig. 57 — Typical device-paralleling arrangements: (a) NOR gates, (b) NAND gates, (c) inverters.

CAPACITIVE LOADING

COS/MOS logic systems should be designed to minimize capacitive loading. Capacitive loading decreases speed and increases power dissipation. In the design of the system, it should be realized that one COS/

MOS unit load imposes a capacitance of 5 picofarads across the output of the COS/MOS circuit.

WIRED-"OR" FUNCTION

In COS/MOS integrated circuits, common busing is not permitted at inverter outputs because of the complementary nature of the basic COS/MOS inverter circuit. With COS/MOS integrated circuits, therefore, the wired-OR function, which is sometimes referred to as the virtual-OR or phantom-OR function, is unrealizable using the outputs of active (gain stage) inverters and gates. Fig. 58 shows the effect of the wired-OR connection on a basic COS/MOS inverter circuit. Results

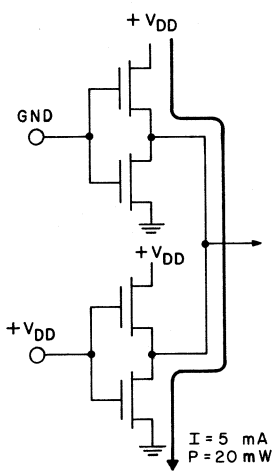


Fig. 58 – Effect of wired-OR connection on the basic COS/MOS inverter circuit. (This connection should be avoided.)

equivalent to those provided by the wired-OR function are obtainable in COS/MOS logic by use of transmission gates and/or functional logic. An example of functional logic is the CD4030A exclusive-OR circuit. The logic diagram for this circuit was shown earlier (in Fig. 42) in the section on **Features and Characteristics of COS/MOS Integrated Circuits.**

COMMON BUSING (THREE-STATE LOGIC)

Transmission-gate logic is used on the outputs of certain COS/MOS registers, such as the CD4034A eight-bit register, to achieve common-bus operation in addition to bidirectional logic gating. The COS/MOS transmission gate output may be a "1", a "0", or an open circuit. Common-bus rules far exceed the "wired-OR" rules for bipolar logic. For example, more than 50 COS/MOS transmission-gate outputs can be wired together while only a small number of bipolar outputs can be tied together because of the greater leakage of bipolar devices. Other standard COS/MOS devices with wired-OR outputs include the quad NAND and quad NOR latches.

In Fig. 59, common bits of four register outputs are common-bused. This type of busing uses the quad transmission gate (CD4016A) approach in which only one output is actively connected to the line at a given instant. The COS/MOS transmission gate can be employed very effectively in common busing of logic levels in complex MSI and custom designs.

POSITIVE/NEGATIVE LOGIC CONVERSION

All data sheets and applications literature for COS/MOS circuits reference positive-logic functionality. Therefore, use of the circuits in

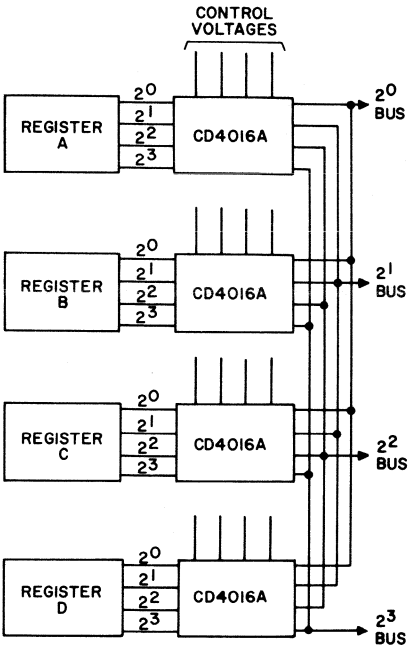


Fig. 59 – Common busing of common bits of four registers using the CD4016A series.

negative-logic systems, while entirely feasible, may lead to some confusion; the interfacing of COS/MOS circuits (positive logic) with p-channel MOS circuits (negative logic) is a common example. The confusion can be avoided by developing an understanding of the relationship between positive and negative logic. This relationship is described below with the aid of a voltage truth table, Table X, in which H represents a high voltage and L a low voltage, X and Y represents inputs, and f(x,y) the output. If the higher level, H, is assigned the value of logical 1, the circuit is said to operate under positive logic. If logical 1 is assigned to L, the lower level, the logic is negative. The corresponding positive and negative logic tables for the voltage truth table of Table X are shown in Table XI.

Table X – Voltage Truth Table

Inputs X	Inputs Y	Output f(x,y)
L	L	H
L	H	L
H	L	L
H	H	L

Possible Logic Assignments	
Positive:	Negative:
H = logical 1	H = logical 0
L = logical 0	L = logical 1

As illustrated in Table X, a positive-logic NOR gate and a negative-logic NAND gate represent two functions reversed in assignment. Therefore, a COS/MOS CD4001A

Table XI – Logic Tables

Positive Logic			Negative Logic		
L = 0 H = 1			L = 1 H = 0		
NOR Function			**NAND Function**		
X	Y	f(x,y)	X	Y	f(x,y)
0	0	1	1	1	0
0	1	0	1	0	1
1	0	0	0	1	1
1	1	0	0	0	1
$f(x,y) = \overline{X \bullet Y}$			$f(x,y) = \overline{X + Y}$		
$= X + Y$			$= X \bullet Y$		

quad two-input NOR gate used in a negative-logic system acts as a quad two-input NAND gate. A CD4011A quad two-input NAND gate acts as a quad two-input NOR gate in a negative-logic system.

The CD4024A is a seven-stage binary counter. In negative logic, the reset acts as a set and will set on a "0". Because the reset acts as a set, the output is all 1's instead of 0's and the counter becomes a down-counter. By inverting all inputs and outputs the counter can be made to operate as it would in a positive-logic system.

Fig. 60 shows how some typical COS/MOS circuit symbols are represented in positive and negative logic systems.

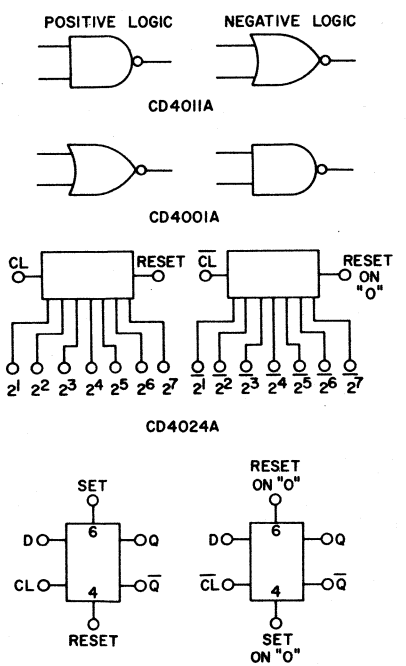


Fig. 60 – Common symbols for COS/MOS devices in positive- and negative-logic systems; symbols apply equally to all device types in a series.

NOISE IMMUNITY

COS/MOS devices function reliably in high-noise environments, such as are found in industrial control and automotive applications, because of their exceedingly high noise immunity. The high noise-immunity characteristics of the devices also make possible the fabrication of extremely inexpensive general-logic-design system packaging configurations.

The exceptionally high ac and dc noise immunity of COS/MOS integrated circuits is attributable to the relatively low output impedances (approximately 600 ohms), moderate-speed operation, steep transfer characteristics, and output voltages within 10 millivolts of V_{DD} when driving other COS/MOS circuits. The high values of noise immunity are achieved with power consumptions in the microwatt range, as compared with much higher (milliwatt) consumptions and lower noise immunities (about 1 volt) for saturated bipolar logic. Because of their high cross-talk noise immunity, COS/MOS circuits are useful in applications requiring long lines or in circuits with closely coupled wiring. COS/MOS circuits are also insusceptible to ground-line noise or noise produced by improper ground returns; therefore, it is not necessary to use large ground or back planes. Similarly, because of the high power-supply noise immunity, complex filtering circuits are not required.

The immunity of a COS/MOS integrated-circuit logic gate to noise signals is a function of many variables, such as individual chip differences, fan-in and fan-out, stray

inductance and capacitance, supply voltage, location of the noise, shape of the noise signal, and temperature. Moreover, the immunity of a system of gates differs from that of any individual gate. Because of the many variables involved, a generalized analysis of the noise immunity of a logic circuit is a complex process. In general, it is more practical to analyze immunity of a system for a specific set of conditions and then to generalize or extrapolate the results to make them applicable to other sets of conditions.

A general analysis of noise immunity involves consideration of immunity to both ac and dc noise. **AC noise** is usually considered to be made up of those noise spikes with pulse widths shorter than the propagation delay of a logic gate. Conversely, **dc noise** spikes are considered to have pulse widths longer than the propagation delay of one gate. AC noise immunity, which varies in direct proportion to dc noise immunity, is largely a function of the propagation delays and output transition times of logic gates and, thus, is a function of the input and output capacitances.

Because COS/MOS logic gates typically change state near 50 per cent of the supply voltage, and because of the steep transfer characteristics exhibited during transitions, exceptionally high input voltages are required to significantly change or falsely switch the output logic state. Typically, then, the input to a COS/MOS logic gate operating at a dc supply voltage of 10 volts may change by 4.5 volts before the output begins to change state. AC noise immunity is also extremely high because of the high static or dc noise immunity and the moderate-speed operation of standard COS/MOS circuits. The high ac noise immunity also implies high immunity to crosstalk noise.

DC noise immunity is defined for COS/MOS integrated-circuit logic gates according to the terms defined in Table XII. Knowledge of these **noise-margin** definitions, which guarantee a noise margin that is 30 per cent of V_{DD}, is useful in designing digital circuits. The **inverter transfer characteristics** shown in Fig. 61, and the output-to-input logic-level characteristics in Figs. 62 and 63, illustrate COS/MOS logic-gate noise immunity. These definitions assure that the logic level at the output of the driving device is recognized as the same logic level at the input to the load device. The dc noise level at the junction is equal to or less than the difference in maximum magnitudes of the output and input logic levels.

Fig. 62 shows guaranteed noise immunity values obtained from the definitions of Table XII for V_{DD} between 3 and 15 volts. At 5 volts, for example, as shown in Fig. 63,

$$V_{NIL} = |0.01 - 1.5| \simeq 1.5 \text{ volts}$$

$$V_{NIH} = |4.99 - 3.5| \simeq 1.5 \text{ volts}$$

At 10 volts,

$$V_{NIL} = |0.01 - 3.0| \simeq 3.0 \text{ volts}$$

$$V_{NIH} = |9.99 - 7.0| \simeq 3.0 \text{ volts}$$

These equations hold for all COS/MOS types except the CD4009A. For this type at 5 volts,

Table XII — Voltage Logic-Level and Noise-Margin Definitions

Voltage Logic Level

V_{OL} Maximum output at low level with no noise at the input. For an inverter, V_{OL}(max) is the output level when the input is tied to V_{DD}, assuming only capacitive loading at the output. For COS/MOS circuits, $V_{OL} = V_{SS} + 0.01$ volt.

V_{OH} Minimum output at high level with no noise at the input. For an inverter, V_{OH}(min) is the output level when the input is grounded, assuming only capacitive loading at the output. For COS/MOS circuits, $V_{OH} = V_{DD} - 0.01$ volt.

V_{ILmax} The maximum input at low level for which the output logic level does not change state.

V_{IHmin} The minimum input at high level for which the output does not change state.

Noise Margin

V_{NIL} Low-level dc noise immunity. The difference in magnitude between the output-voltage level of the driving device in the low-level state (V_{OL}) and the maximum input low-level voltage recognized by the driven load device (V_{ILmax}).
$V_{NIL} = |V_{OL} - V_{ILmax}|$

V_{NIH} High-level dc noise immunity. The difference in magnitude between the output-voltage level of the driving device in the high-level state (V_{OH}) and the minimum input high-level voltage recognized by the driven load device (V_{IHmin}).
$V_{NIL} = |V_{OH} - V_{IHmin}|$

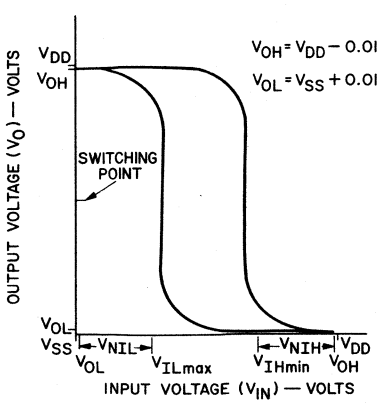


Fig. 61 — Inverter transfer characteristic.

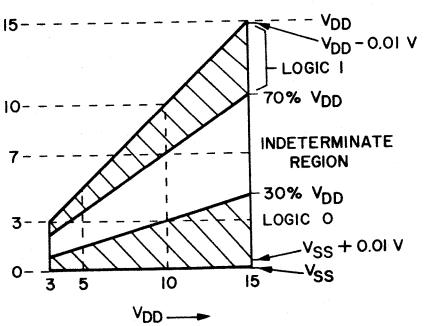


Fig. 62 — Guaranteed noise-immunity values.

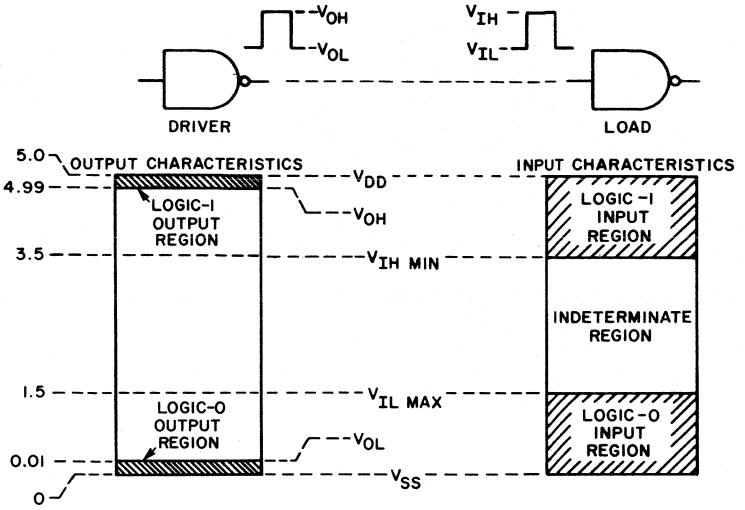


Fig. 63 — Output to input logic-level characteristics.

$V_{NIL} = |0.01 - 1.0| \simeq 1.0$ volt

$V_{NIH} = |4.99 - 3.5| \simeq 1.5$ volts

At 10 volts,

$V_{NIL} = |0.01 - 2.0| \simeq 2.0$ volts

$V_{NIH} = |9.99 - 7.0| \simeq 3.0$ volts

The 30-per-cent noise margins apply to all COS/MOS types except the CD4009A, which has a low-level noise-immunity margin of 20 per cent because V_{IL} = 1 volt at V_{DD} = 5 volts and V_{IL} = 2 volts at V_{DD} = 10 volts; the high-level noise immunity V_{NIH} is 30 per cent, the same as for all other COS/MOS types.

Inverter transfer characteristics change very little with changes in ambient temperature over the temperature ranges allowed for COS/MOS circuits in both plastic and ceramic packages. Because of the excellent temperature stability of the transfer characteristic, the noise immunity changes no more than 0.3 volt over the -55°C to +125°C temperature range with V_{DD} less than or equal to 10 volts.

INTERFACING COS/MOS WITH OTHER LOGIC FORMS

Proper interfacing between different logic families requires that the circuits selected operate at a common supply voltage and display logic-level compatibility. In addition, the devices must maintain safe power-dissipation levels and good noise immunity over the specified operating-temperature range.

Of great significance is the ease of interfacing the COS/MOS CD4000A series with the widely used TTL and DTL logic families. The wide operating-voltage range of

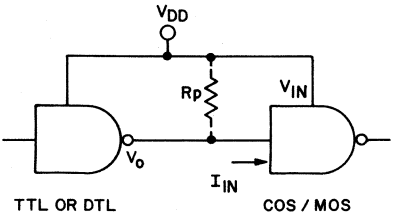
COS/MOS devices also permits direct interface with HTL (High-Threshold-Logic) and p- and n-channel MOS logic circuits. Interfaces with ECL systems (0- and 5-volt supplies) are power-supply compatible but require logic-level conversion.

Saturated-Bipolar Logic

A need arises to interface COS/MOS logic with higher-speed, saturated bipolar logic when system logic speeds exceed approximately 10 MHz. Optimum efficiency in system design is achieved by directly but alternately interfacing COS/MOS circuits and DTL or TTL circuits; i.e., taking full advantage of the superior COS/MOS logic characteristics at lower logic speeds and the high-speed capability of saturated bipolar logic when required.

Bipolar Driving COS/MOS

Fig. 64 shows a TTL or DTL gate directly driving one COS/MOS device input. Limit values of bipolar drive parameters are shown, as are the limit parameters of the driven COS/MOS device. Examination of Fig. 64 indicates that for the bipolar-output logic-0 case, the COS/MOS device is safely driven with a safety (noise) margin of 1.1 volts (1.5V-0.4V). The net effect is a reduction of noise margin from 30 to 22 per cent of V_{DD} when compared with COS/MOS driving COS/MOS. For the logic-1 case of TTL driving COS/MOS, a borderline situation exists. The minimum no-load logic-1 TTL output is 3.6 volts, while the COS/MOS minimum logic 1 input voltage required is 3.5 volts. This interface is valid, but has essentially



Logic "0" Case
V_{DD} max = 5.5V
V_o max = .4 (10 pA load)
V_{IN} min = 1.5V for guaranteed switching
I_{IN} = 10 pA

Logic "1" Case (TTL only)
V_{DD} min = 4.5V
V_o max = 3.6V
V_{IN} min = 3.5V for guaranteed switching
I_{IN} = 10 pA

Logic "1" Case (DTL only)
V_{DD} min = 4.5V
V_o min = 4.5V
V_{IN} min = 3.5V for guaranteed switching
I_{IN} = 10 pA

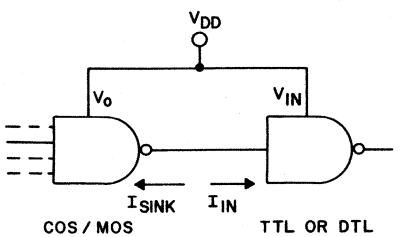
Fig. 64 – TTL or DTL gate directly driving one COS/MOS device input.

no noise margin (0.1 volt). Therefore, it is recommended that an external **pull-up resistor**, R_p, be used to guarantee the interfacing of TTL with COS/MOS; V_o would then be equal to V_{DD}. R_p affects the logic-0 interface condition in that V_o max is increased. Determination of an optimum value for R_p requires consideration of fan-out, maximum TTL device current, V_o max, TTL device leakage in the high state, power consumption, and propagation delay. Appropriate network equations can be developed to permit calculation of an optimum value of R_p for a given TTL or DTL logic family. The logic-1 case of a bipolar DTL circuit driving a COS/MOS circuit is a highly satisfactory inter-

face and full COS/MOS noise margin is unaffected. Most bipolar logic families have open-collector-output family members for use in phantom-OR logic connections. By utilizing these devices, optimum values of the external resistor R_p can be selected for specific speed and noise-margin system requirements.

COS/MOS Driving Bipolar

Fig. 65 shows one COS/MOS gate driving one TTL or DTL gate input. When the COS/MOS output is a logic 1, the TTL or DTL load acts as a reverse-biased diode; maximum



Logic "1" Case

V_{DD} min = 4.5V
V_o min = 4.4V
I_{IN} = 40 μA max.
V_{IN} max. required = 2.9V

Logic "0" Case

V_{DD} min = 4.5V
V_o = .8V @ 1.8 mA Sink Current (CD4001)
I_{IN} max = 1.6 mA
V_{IN} max = .8V

V_o = .8V @ 7 mA Sink Current (CD4009/CD4010)

Fig. 65 — COS/MOS gate driving TTL or DTL gate input.

load current is 40 microamperes at a minimum COS/MOS output voltage of 4.4 volts. Because the minimum required TTL or DTL input voltage is 2 volts, greater than 50 per cent noise immunity exists.

For the logic-0 TTL or DTL input condition, a maximum input voltage of 0.8 volt is required at 1.6 milliamperes of sink current. Driving with 0.8 volt permits essentially no noise immunity; therefore, a 0.4-volt drive is recommended. Table XIII shows COS/MOS output-sink-current capability at 0.4 and 0.8 volt. Only the CD4009A and CD4010A buffers can drive TTL or DTL inputs directly with the simple logic connections shown in Fig. 66(a). At an output of 0.4 volt, two TTL or DTL gates can be driven; at an output of 0.8 volt, four gates can be driven.

Increased sink-current capability of COS/MOS NOR devices can be achieved by paralleling input and output connections of multiple-input gates, as shown in Fig. 57. Fig. 66(b) shows a quad two-input NOR gate (with inputs paralleled) driving one DTL or TTL load. This connection provides 1.8 milliamperes at 0.8 volt. Fig. 66(c) shows one COS/MOS gate driving a TTL or DTL load at 1.8 milliamperes and 0.4 volt. In Fig. 66(c), four n-channel transistors are paralleled as shown in the schematic diagram of Fig. 67. In a similar fashion, both inputs and outputs of three CD4007A inverters may be paralleled to drive one DTL or TTL load.

Low-power TTL logic devices (54 L or 74 L series) can be driven directly by most COS/MOS devices. The sink-current requirement of these devices is only 0.18 milliampere per bipolar input. Table XIII shows fan-out calculations for eight COS/MOS types. For example, one CD4000A device output will drive three 54 L loads at 0.4 volt.

Table XIII — Current-Sinking Limits of COS/MOS Devices

Type	Description	Sink Current (mA)	
		V_{OL} = 0.4 V	V_{OL} = 0.8 V
CD4000A	Dual 3-input NOR Gate Plus Inverter	0.40	0.8
CD40001A	Quad 2-input NOR Gate	0.40	0.8
CD4002A	Dual 4-input NOR Gate	0.40	0.8
CD4007A	Dual Complementary Pair plus Inverter	0.6	1.2
CD4009A	Inverting Hex Buffer	3.0	6
CD4010A	Noninverting Hex Buffer	3.0	6
CD4011A	Quad 2-input NAND Gate	0.2	0.4
CD4012A	Dual 4-input NAND Gate	0.1	0.2

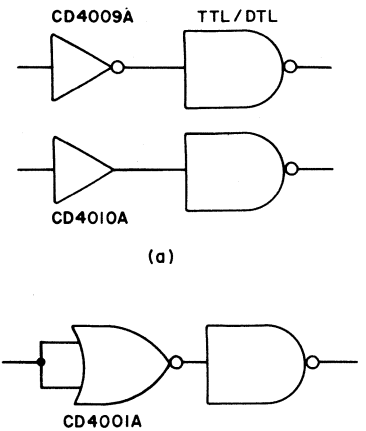


Fig. 66 — Sink-current enhancement connections for COS/MOS driving TTL and DTL; circuits apply equally to all device types in a series.

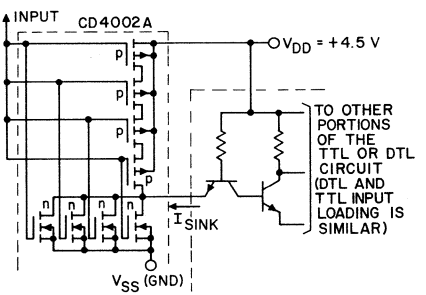
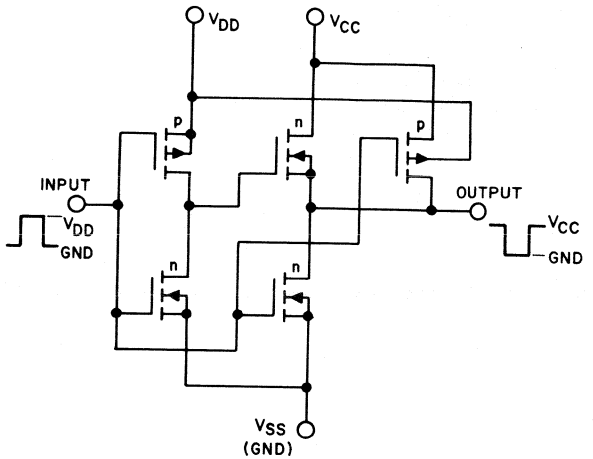


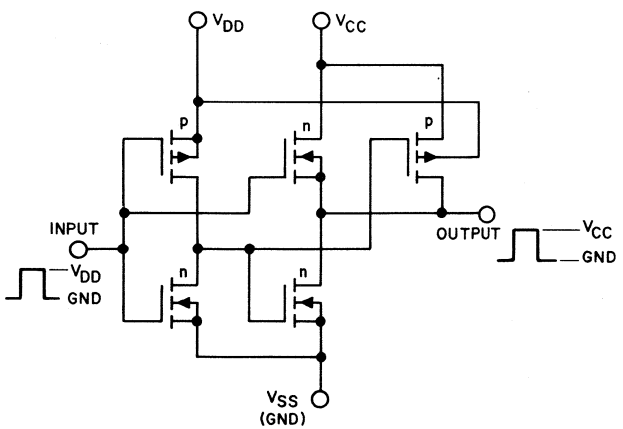
Fig. 67 — COS/MOS circuit with paralleled inputs driving TTL or DTL circuit.

Level Shifting

The two COS/MOS buffers (CD4009A and CD4010A) are designed as **level shifters** as well as high-sink-current drivers. This important feature permits operation of COS/MOS logic at supply-voltage values up to +15 volts and direct interface with TTL or DTL at +5 volts. Fig. 68 shows the schematic



(a)



CONFIGURATION (EACH CIRCUIT):
HEX COS/MOS TO DTL OR TTL CONVERTER (NON-INVERTING)

WIRING SCHEDULE:
CONNECT V_{CC} TO DTL OR TTL SUPPLY
CONNECT V_{DD} TO COS/MOS SUPPLY

(b)

Fig. 68 – Schematic diagrams of the (a), CD4009A and (b) CD4010A.

diagrams of the CD4009A and CD4010A buffers; V_{DD} is the COS/MOS logic-level voltage and V_{CC} is the +5-volt TTL or DTL connection. Fig. 69 shows the logic-interface connections for logic-level conversion. The system advantage of this scheme is manifested in the increased logic speed of COS/MOS circuits when operated at higher speeds than would be possible in an all +5-volt system.

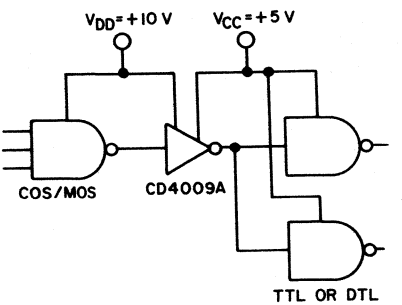
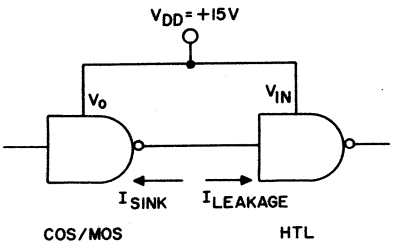


Fig. 69 – Logic-interface connections for logic-level conversion.

High-Threshold Logic

HTL (High-Threshold Logic) operates with a 15 ± 1-volt supply and achieves the 45-per-cent noise immunity typical of COS/MOS devices by utilization of a zener diode (6.7 volts) at the circuit inputs. HTL outputs are driven from an n-p-n switching transistor and a 15-kilohm pull-up resistor. Therefore, when HTL circuits drive COS/MOS circuits, the inherently high noise immunity (typically 45 per cent of supply voltage) of both devices is maintained. The COS/MOS-HTL interface requires a 1.2-milliampere sink-current capability for the COS/MOS output circuit. Fig. 70 illustrates this interface and shows the characteristics for both the logic-1 and the logic-0 COS/MOS-output cases. Both the



Logic – 1 Case
V_{output} (min) = 14.99V
V_{IN} (min) = 8.5V

Logic – 0 Case
V_o (max) = 0.8 V, 1 = 16 mA (CD4009A or CD4010A)
$I_{LEAKAGE}$ (max) = 2 μA
V_{IN} (max) = 6.5V
I_{SINK} (max) = 1.2 mA

I = 1.2 mA (CD4001)

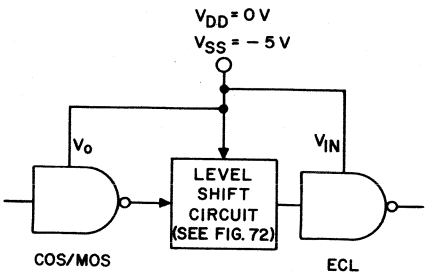
Fig. 70 – COS/MOS and HTL interface.

COS/MOS and HTL circuits operate from a common 15-volt supply. For the COS/MOS logic-1 output case of Fig. 70, high noise immunity is achieved by using the CD4009A or CD4010A buffer.

Emitter-Coupled Logic

COS/MOS and ECL (Emitter-Coupled Logic) logic forms can be operated from a common -5 ± 1-volt supply. However, level-shift interface circuits are required in both directions.

Fig. 71 illustrates the COS/MOS-to-ECL logic-1 and logic-0 level interface requirements. Fig. 72(a) illustrates a simple voltage-divider interface circuit. The calculation of the values of resistors R1 and R2 is based on COS/MOS source- and sink-current capability and ECL input loading. This interface suffers from



	Logic 1	Logic 0
V_o	0V	-5V
V_{IN}	-0.8V	-1.6V

Fig. 71 — COS/MOS and ECL interface.

poor temperature tracking and low speed. The active level translator of Fig. 72(b) has a high speed capability and good temperature tracking.

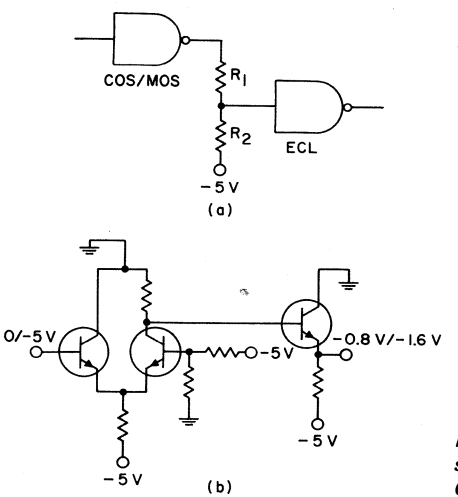
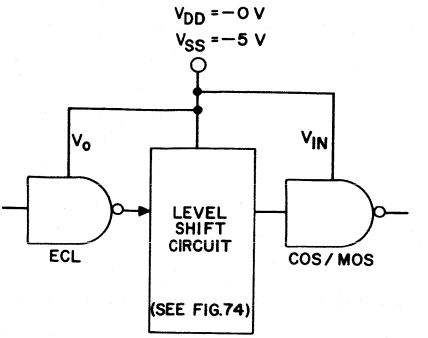


Fig. 72 — (a) COS/MOS and ECL voltage-divider interface circuit; (b) active level translator.

An active interface circuit is required to shift from ECL output logic levels to COS/MOS logic levels. Figs. 73 and 74 illustrate logic-



	Logic 1	Logic 0
V_o	-0.8V	-1.6V
V_{IN}	-0.8V	-4.2V

Fig. 73 — Logic interface required to shift from ECL output logic levels to COS/MOS logic levels.

interface and level-shift circuits, respectively. An important consideration in these interfaces, as well as in the COS/MOS-to-ECL interface of Figs. 71 and 72, is operation from the common -5-volt supply.

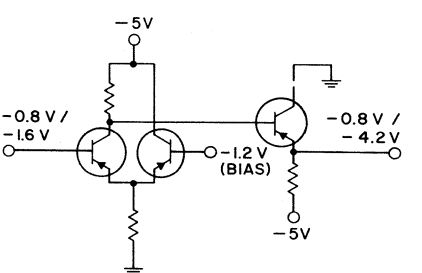


Fig. 74 — Level-shift circuit required to shift from ECL output logic levels to COS/MOS logic levels.

IC level shifters that translate between TTL or DTL logic levels and ECL logic levels are commercially available. Both +5-volt and -5-volt power-supply voltages must be provided when these level shifters are used. The COS/MOS CD4009A or

CD4010A hex buffers may be required to drive the TTL-to-ECL level-shifter IC's. In this case, a third power supply (up to +15 volts) may be used to power the COS/MOS logic circuits.

P-Channel MOS

P-channel MOS-transistor logic levels are -6 volts for low-threshold and -15 volts for high-threshold types. Direct interface with COS/MOS logic circuits is achieved by operating the COS/MOS circuit at a V_{DD} of zero volts and a V_{SS} of either -6 or -15 volts. COS/MOS positive and negative logic considerations, as explained earlier in the discussion on **Positive/Negative Logic Conversion**, are helpful in converting the positive-logic functionality of COS/MOS devices to the p-channel MOS-circuit negative-logic convention.

N-Channel MOS

N-channel MOS-transistor logic levels are positive and within the voltage range of COS/MOS devices; direct interface is therefore possible.

CLOCKING REQUIREMENTS

All sequentially operated COS/MOS integrated circuits require a single-phase clock. The amplitude of the clock pulse should be equal to the single power-supply voltage V_{DD}. Fig. 75 shows the clock-edge requirements for all flip-flops, shift registers, counters, and latches included in the CD4000A series of COS/MOS integrated circuits.

Clock-edge rise and fall times should not exceed 15 microseconds

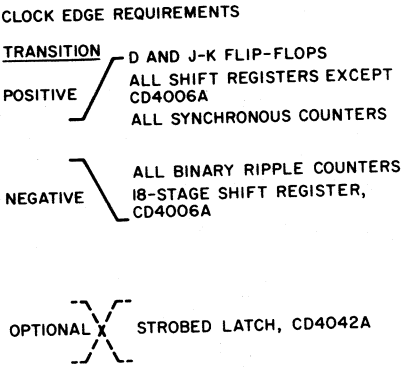


Fig. 75 — Clock-edge requirement for CD4000A-series COS/MOS integrated circuits.

because of circuit cascading considerations, as explained in the next section. Minimum clock pulse width and maximum operating frequency are functions of the supply voltage and the type of device.

CASCADING CONSIDERATIONS

When sequential COS/MOS circuits, such as flip-flops and shift registers, are to be connected in cascade, the designer must take care that data are not lost in the transfer between different devices. Variations in the range of input switching levels and flip-flop time constants may result in a loss of data.

Input Switching Levels

The input switching level of an active COS/MOS circuit has a 4-volt range for operation from a 10-volt power supply, as shown earlier in Fig. 55. This range of switching levels is the result of the range of threshold variations of present MOS technology. These variations present no

problem in dc logic usage; they can, however, affect error-free cascading of shift register stages.

The range of switching levels can cause loss of data between certain synchronously clocked sequential circuits, as shown in Fig. 76. For example, if two or more COS/MOS flip-flops (CD4013A or CD4027A) or shift registers (CD4006A, CD4014A, CD4015A, or CD4021A) are cascaded, the clock rise time (t_rCL) should be made less than the total of the fixed propagation delay plus the output transition time, as determined from the device data sheet for the specific capacitive loading condition in effect.

In the CD4031A 64-bit static shift register, this problem is avoided by use of a delayed clock output.

Time Constants

The range of COS/MOS switching points also affects the time constants of multivibrator circuits. Compensation techniques used with the circuits are discussed later in the section on **Astable and Monostable Multivibrators.**

POWER–SOURCE CONSIDERATIONS

In determination of the power source for a COS/MOS logic system, the first step is to ascertain the total power requirements of the over-all system. This factor significantly affects the regulation and filtering requirements and also indicates whether battery operation is feasible.

Calculation of System Power Requirements

Guidelines have been developed to assist the designer in estimating system power. The guidelines take into account the ultra-low power dissipation of COS/MOS devices in the quiescent state and the increased power dissipation with increased

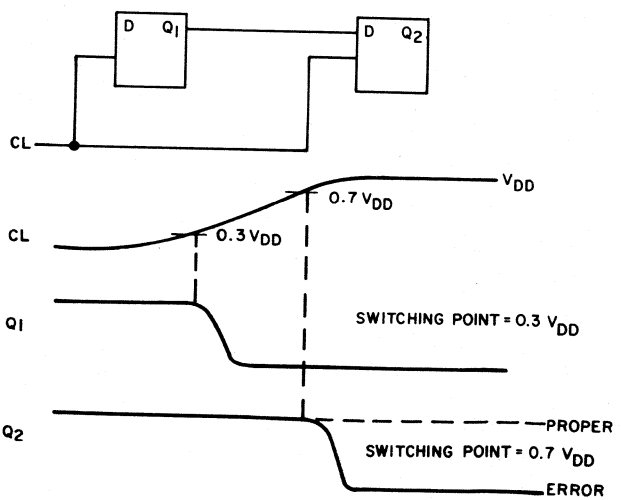


Fig. 76 – Error effect that results from a slow clock in cascaded circuits.

loading (primarily capacitive) and switching rate. Total COS/MOS system power is the sum of the quiescent power plus the dynamic power, as follows:

$$P_{Total} = P_{Quiescent} + P_{Dynamic}$$

As the first step in calculating system power, the quiescent power dissipation of all devices used is summed. Individual device dissipation may be obtained from COS/MOS data sheets or from the tables of quiescent power given earlier in this Manual in the section concerning **Features and Characteristics of RCA COS/MOS Integrated Circuits.**

Because quiescent power dissipation is equal to the product of quiescent device current and supply voltage, the total quiescent dissipation (either typical or maximum) may be obtained by adding all quiescent device currents and multiplying this sum by the value of the supply voltage, V_{DD}. The quiescent current for a device is shown in the data sheets at supply voltages of 5 and 10 volts only; the quiescent device current can be interpolated for other values of supply voltage because the current curve approximates a linear relationship with voltage.

As the second step in calculating system power, the dynamic power dissipation is determined for each device. These data are available in the dynamic dissipation versus frequency curves shown in this Manual in the section concerning **Features and Characteristics of RCA COS/MOS Integrated Circuits** or on the data sheet for the device in question. The individual device values are summed to yield total dynamic power dissipation.

Total system power is then determined by adding together the total quiescent and the total dynamic power dissipation. In high-speed logic systems, i.e., systems with speeds of 1 MHz or more, most of the dissipation is dynamic and quiescent dissipation may be neglected.

Regulation

COS/MOS devices exhibit reliable switching properties over a wide range of power-supply voltages. Specifically, CD4000A COS/MOS devices operate reliably and with high noise immunity as long as the power-source voltage ($V_{DD} - V_{SS}$) is greater than 3 volts and less than 15 volts. This statement implies that an unregulated supply may be used provided that maximum voltage limits are not exceeded and that system speed is no greater than the speed which can be supported by the COS/MOS device operating at the lowest value of V_{DD} expected from the unregulated supply. Maximum system speed, then, is dictated by the minimum power-source excursion.

To establish the extent of regulation required, the power-supply designer must first determine the maximum operating frequency required of his system. Usually one device in the system is the limiting element in the chain. As pointed out earlier in the section on **Features and Characteristics of RCA COS/MOS Integrated Circuits**, a minimum value of supply voltage ($V_{DD} - V_{SS}$) as a function of both required device speed and the number of unit loads driven can easily be determined. A

nominal power-supply voltage midway between the minimum supply-voltage value and 15 volts is determined. The percentage of permissible power-supply regulation is then easily calculated.

As an example of the use of the above considerations, the maximum clock input frequency (toggle rate) of a CD4013A flip-flop is typically 4 MHz at 3 unit loads (C_L = 15 picofarads) and a minimum supply voltage of +5 volts. (These values were taken from data on the CD4013A (Fig. 52) given in the section on **Features and Characteristics of RCA COS/MOS Integrated Circuits.** By selection of a nominal +10-volt supply, ±50-per-cent maximum regulation can be tolerated, thus guaranteeing the 4-MHz operation.

Battery Operation

Because of their ability to operate over a wide voltage range at a very low level of current drain, COS/MOS logic circuits can be operated directly from inexpensive batteries having a wide voltage excursion from "beginning" to "end" of life. Additionally, the very high noise immunity of COS/MOS devices is an advantage in battery operation because the internal impedance of batteries is often greater than the internal impedance of most power supplies.

The low power dissipation of COS/MOS devices offers another important advantage where battery operation is required. COS/MOS logic systems can be effectively nonvolitile; i.e., they will not change state during long periods of time. In essence, then, the battery powering the devices behaves as a shelf-life battery for quiescent system operation; holding voltages can be as low as 2 volts. The system designer can think of this COS/MOS feature as a quiescent non-volatile memory capability in planning various system applications.

Automotive batteries of a 12-volt nominal rating can directly drive COS/MOS logic circuits. Care must be taken, as with most other electronic devices, to protect COS/MOS devices from high-voltage transients resulting from open-circuited battery terminals; transients as high as 100 volts can arise from the high electric field in an automobile generator. The usual means of protection is the zener-diode protection circuit.

Zener-Diode-Reference Operation

Operation from zener-diode references not only protects COS/MOS devices from momentary line transients, but also can provide an effective power-supply source from dc sources exceeding 15 volts, such as a 28-volt aircraft supply. The zener-diode source is also effective when accurate digital-to-analog converters are designed using COS/MOS devices.

Proper design of zener regulators for COS/MOS logic operations must take into account the transient nature of most COS/MOS current-drain requirements. Current drains in excess of the microampere quiescent currents are an integral sum of the switching-transient currents of the COS/MOS devices. Knowledge of peak currents (I_p), switching fre-

quency, and current rise and fall times must be judiciously used in calculating the R and C of the zener regulating circuit shown in Fig. 77.

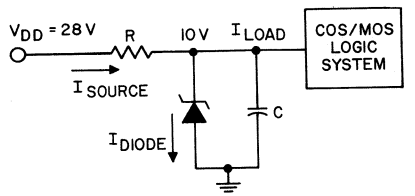


Fig. 77 — Zener regulating circuit.

In complex-logic systems, estimates of R and C from a knowledge of the average system frequency and the switching-transient characteristics of COS/MOS devices may be easily made. The use of this knowledge in some arbitrary laboratory adjustment usually quells the transient-current problem quickly. The key here is awareness of the purely transient nature of most COS/MOS loads.

Filtering

COS/MOS-system power supplies need be filtered only to the extent that the magnitude of the ripple, on a peak basis, does not drop below the minimum voltage required to support the switching frequency of the COS/MOS devices used.

The job of the designer is, then, to determine the minimum instantaneous voltage permissible that will support the system switching frequency and from that minimum voltage to determine the maximum regulation and/or filtering required for the specified supply voltage. As long as the amplitude of the ripple does not exceed the maximum noise-immunity range, COS/MOS circuits will continue to operate as if no ripple were present. Fig. 78 shows a plot of peak-to-peak ripple versus maximum operating frequency at supply voltages of 5 and 10 volts.

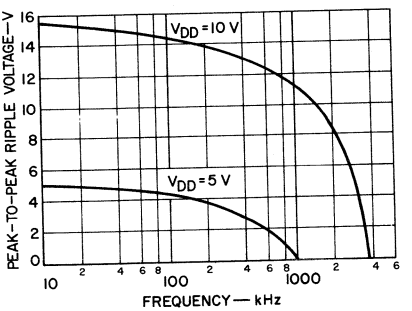


Fig. 78 — Peak-to-peak ripple versus maximum operating frequency for a typical COS/MOS A-series circuit at supply voltages of 5 and 10 volts.

The curves show that ripple does not affect the operation of the COS/MOS device except in those instances where ripple approaches the 100-percent mark.

Filtering requirements over and above those described need only be related to system-power-bus "cleanliness" as determined by over-all system performance specifications. COS/MOS logic is outstanding in this respect, requiring minimum filter-design expense, as opposed to high-current-drain logic forms which require costly filter design.

Astable and Monostable Multivibrators

COS/MOS gates provide cost and size reductions in multivibrator circuits because their high input impedance makes it possible to obtain large time constants without the use of large capacitors. This section describes several techniques which may be used to compensate for the normal threshold variation of MOS devices in the design of stable multivibrator circuits. Operating frequencies up to 2 MHz and more can be attained with the CD4000A series. The circuits shown can be formed by use of the individual inverters in various COS/MOS IC's, such as the CD4000A, CD4001A, CD4002A, or CD4007A.

ASTABLE CIRCUITS

Fig. 79(a) shows an astable multivibrator circuit that uses two COS/MOS NOR gates as inverters; NAND gates or ordinary inverters may be substituted for the NOR gates. Fig. 79(b) shows the waveforms for the circuit of Fig. 79(a). This simple circuit requires only one resistor and one capacitor.

Basic Circuit Operation

When waveform (1) at the output of inverter B is in a high or "1" state, capacitor C_{tc} becomes positively charged. As a result, the input to inverter A is high, and its output is low or "0". Resistor R_{tc} is returned to the output of inverter A to provide a path to ground for discharge of C_{tc}. As long as the output of inverter A is low, the output of inverter B is high. As capacitor C_{tc} discharges, however, the voltage generated [waveform (2) in Fig. 79(b)] approaches and passes through the transfer-voltage point of inverter A. At the instant that this crossover occurs, the output of A becomes high; as a result, the output of B becomes low and capacitor C_{tc} is charged negatively (or low). Resistor R_{tc}, connected to the output of A, then provides a charge path for the supply voltage. Capacitor C_{tc} begins to charge to this voltage. Again, the voltage approaches and passes through the transfer-voltage point of inverter A. At that instant,

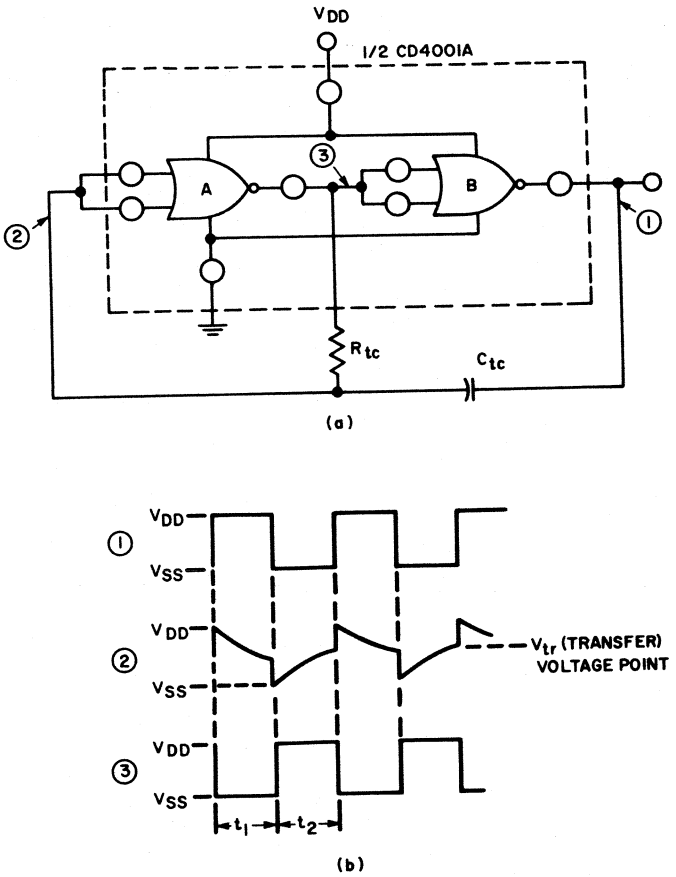


Fig. 79 – (a) Astable multivibrator circuit; (b) voltage waveforms.

the circuit again changes state (the output of A becomes low and that of B high), and the cycle repeats.

Because input-diode protection circuits like the one shown in Fig. 80 are included in COS/MOS IC's, the generated drive waveform is clamped between V_{DD} and V_{SS}. Consequently, the time to complete one cycle is approximately 1.4 times the RC time constant because one time constant is used to control the switching of both states of the multivibrator circuit. Switching occurs when the charge or discharge reaches the transfer-voltage level, or when the time period reaches 70.7 per cent of its discharge. As shown in waveform (2) of Fig. 79(b), the transfer-voltage point V_{tr} is the same for t_1 and t_2. The time period T for one cycle can be computed as follows:

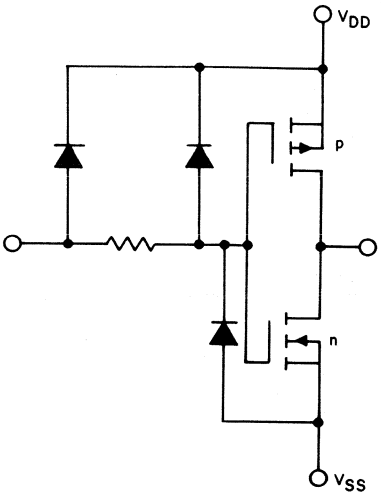


Fig. 80 — Diode protection circuit.

$$T = t_1 + t_2$$

$$t_1 = -RC \ln \frac{(V_{DD} - V_{tr})}{V_{DD}}$$

$$t_2 = -RC \ln \frac{V_{tr}}{V_{DD}}$$

$$T = -RC \left[\ln \frac{(V_{DD} - V_{tr})}{V_{DD}} + \ln \frac{V_{tr}}{V_{DD}} \right] \qquad (14)$$

If the time constant is assumed to be 1 x 10^{-6} second and the transfer voltage V_{tr} is allowed to vary from 33 to 67 per cent of V_{DD}, the period T varies from 1.4 microseconds at a value of V_{tr} equal to half of V_{DD} to 1.5 microseconds at either the 33- or 67-per-cent value of V_{DD}. Therefore, the maximum variation in the time period T is only 9 per cent with a ±33-per-cent variation in transfer voltage from unit to unit.

Multivibrator operation can be made independent of supply-voltage variations by use of a resistor R_S in series with the input lead to inverter A, as shown in Fig. 81(a). The value of this resistor should be at least twice as large as that of resistor R_{tc} to allow the voltage waveform generated at the junction of R_S, R_{tc}, and C_{tc} to rise to $V_{DD} + V_{tr}$. The waveform is still clamped between V_{DD} and V_{SS}, as shown by the waveforms in Fig. 81(b). The use of

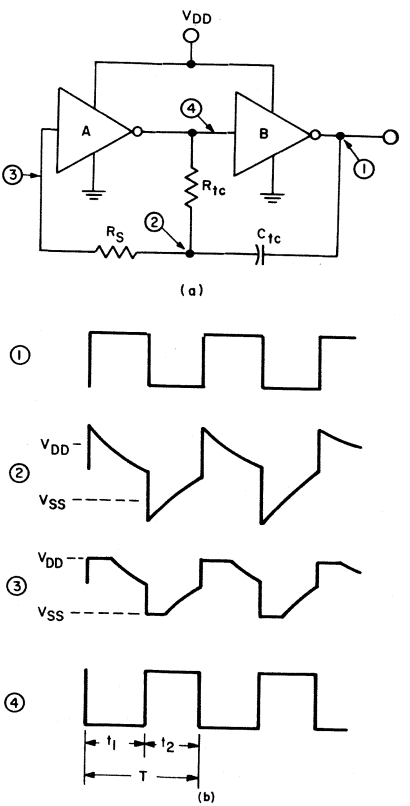


Fig. 81 — (a) COS/MOS inverter with resistor in series with one input to make circuit independent of supply-voltage variations; (b) voltage waveforms.

resistor R_S provides several advantages in the circuit. First, because the RC time constant controls the frequency, the over-all maximum variations in the time period are reduced to less than 5 per cent with variations in transfer voltage, as determined by the following equation:

$$T = -RC\left[\ln\frac{V_{tr}}{(V_{DD}+V_{tr})} + \ln\frac{(V_{DD}-V_{tr})}{2V_{DD}-V_{tr}}\right] \quad (15)$$

Resistor R_S also makes the frequency independent of supply-voltage variations. Table XIV shows data measured on typical units with and without the resistor.

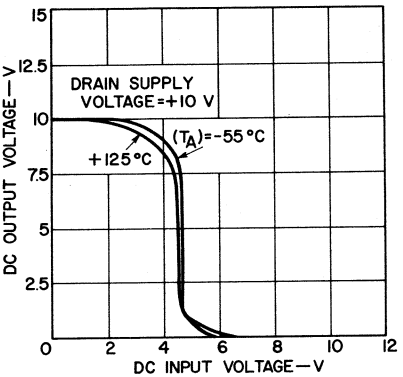


Fig. 82 — Typical COS/MOS transfer characteristic as a function of temperature.

Table XIV — Frequency variations of astable multivibrator with and without series resistor

Unit No.	V_{tr} @ V_{DD} = 10V (V)	Period Without Rs - (ms)			Period With Rs - (ms)		
		V_{DD} = 6V	V_{DD} = 10V	V_{DD} = 14V	V_{DD} = 6V	V_{CC} = 10V	V_{CC} = 14V
2	4.77	0.735	0.66	0.645	1.04	1.00	1.02
6	5.78	0.715	0.665	0.63	1.06	1.04	1.03
11	5.58	0.695	0.66	0.625	1.03	1.02	1.03
13	5.00	0.70	0.665	0.64	1.03	1.01	1.02
20	5.56	0.70	0.665	0.64	1.04	1.03	1.03

R_{tc} = 0.4 megohm, C_{tc} = 1000pF, R_S = 0.8 megohm

Transfer Characteristic

Fig. 82 shows a typical transfer characteristic as a function of temperature. It can be seen that there is very little change in the characteristic from low to high temperature. Because the multivibrator can also tolerate changes in the transfer characteristic without frequency instability, it requires no thermal compensation. The frequency at −55°C is the same as at +125°C. Table XV shows data measured on typical units at temperature extremes. The astable multivibrator shown in Fig. 79 can be gated ON and OFF by use of a NOR or NAND gate as the first inverter, as shown in Fig. 83.

Table XV — Frequency variations of astable multivibrator at temperature extremes

	Period (ms)					
	V_{DD} = 6V		V_{DD} = 10V		V_{DD} = 14V	
Unit No.	-55°C	+125°C	-55°C	+125°C	-55°C	+125°C
2	1.04	1.04	1.02	1.01	1.03	1.02
6	1.06	1.07	1.06	1.04	1.04	1.03
11	1.03	1.03	1.04	1.02	1.04	1.01
13	1.02	1.02	1.02	1.02	1.03	1.01
20	1.04	1.03	1.04	1.03	1.04	1.02

R_{tc} = 0.4 megohm, C_{tc} = 1000pF, R_S = 0.8 megohm

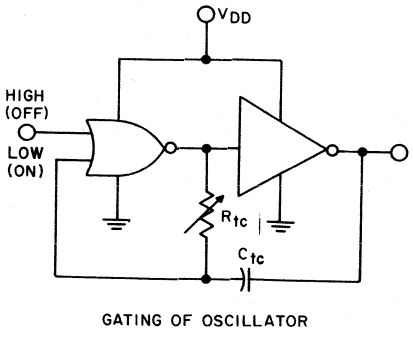


Fig. 83 — Astable multivibrator with NOR- or NAND-gate first inverter to permit gating of the multivibrator

Compensation for 50-per-cent Duty Cycles

The variation in transfer voltage described above affects the output-pulse duty cycle, as shown in Fig. 84.

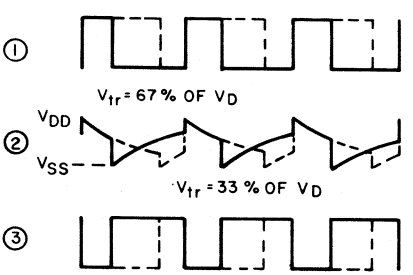


Fig. 84 — Effect of transfer voltage on multivibrator frequency.

A true square-wave pulse is obtained only when the transfer voltage occurs at the 50-per-cent point. However, the duty cycle can be controlled if part of the resistance in the RC time constant is shunted out with a diode, as shown in Fig. 85. Because adjustment of this diode shunt to obtain a specific pulse duty factor causes the frequency of the circuit to vary, a

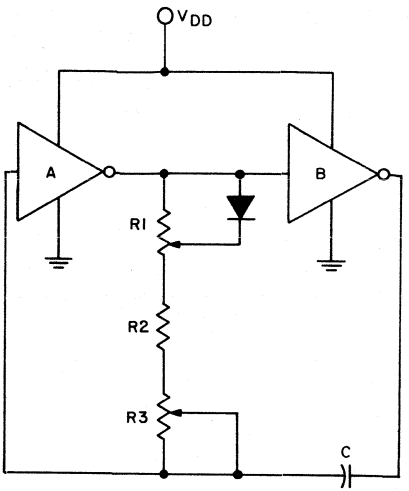


Fig. 85 — Astable multivibrator with duty-cycle control.

frequency-control resistor, R3, is added to compensate for this variation. It may also be necessary to reverse the diode to obtain the desired duty factor. The frequency of any of the circuits shown can be made variable by use of a potentiometer in place of resistor R_{tc}.

MONOSTABLE CIRCUITS

Fig. 86(a) shows a basic one-shot circuit that uses a single RC time constant. This circuit operates well provided it is adjusted to the COS/MOS unit used. If no adjustment is made, period T can vary by as much as −40 per cent to +60 per cent as the transfer voltage varies by ±33 per cent. These variations are illustrated in the waveforms of Fig. 86(b).

Compensated Circuit

Fig. 87 shows a compensated monostable multivibrator circuit that

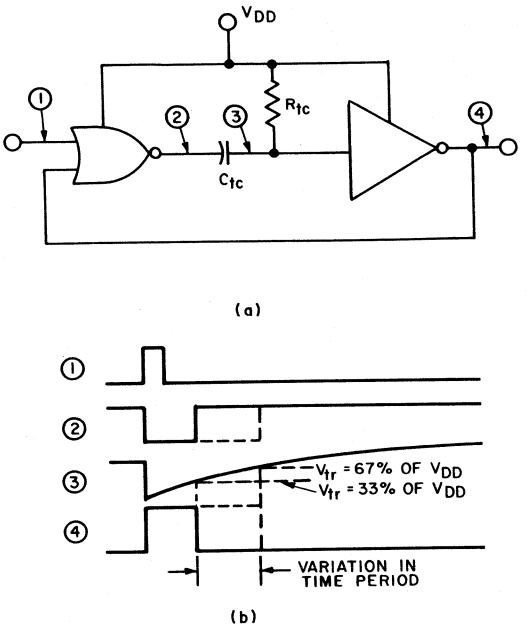


Fig. 86 – (a) Basic one-shot multivibrator circuit; (b) circuit waveforms.

can be triggered with a negative-going pulse (V_{DD} to ground). In the quiescent state, the input to inverter A is high and the output low; therefore, the output of inverter B is high. When a negative-going pulse or spike is introduced into the circuit, as shown in the waveforms of Fig. 88, capacitor C1 becomes negatively charged to ground and the output of inverter A becomes high. Capacitor C2 then charges to V_{DD} through diode D1 and inverter A; the output of inverter B becomes low. As capacitor C1 discharges negatively, it charges through resistor R1 to V_{DD}

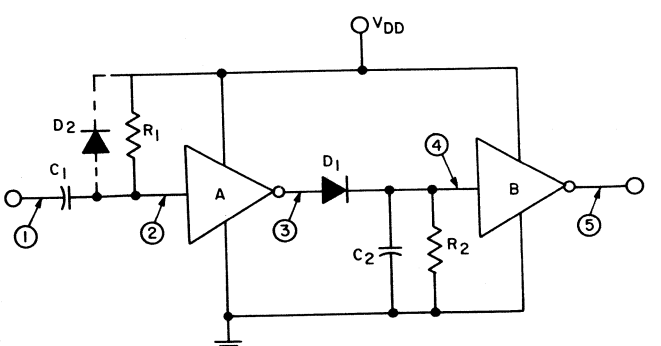


Fig. 87 – Compensated monostable-multivibrator circuit.

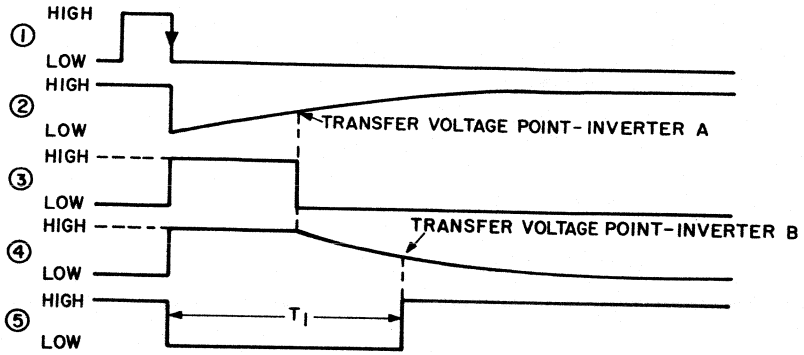


Fig. 88 — Voltage waveforms for the circuit of Fig. 87 with negative-going trigger pulse applied.

[waveform (2)]. The output of inverter A remains high until the voltage waveform generated by the charge of C1 passes through the transfer voltage of inverter A; at that instant, its output becomes low. Diode D1 temporarily prevents the discharge of capacitor C2 which was charged when inverter A was high [waveform (3)]. Capacitor C2 then begins to discharge to ground through resistor R2 [waveform (4)]. The output of inverter B remains low until the waveform generated by the discharge of C2 passes through the transfer-voltage point of inverter B; at that point, the output returns to its high state [waveform (5)]. The advantage of using two inverters fabricated on the same chip is that they have similar transfer voltages. When two equal RC time constants are used (R1C1 equals R2C2), the effects of variations in transfer voltage from device to device are effectively cancelled out, as shown in Fig. 89. By use of Eq. (14), derived for the astable oscillator, it can be shown that the maximum variation in transfer voltage in the time period T is less

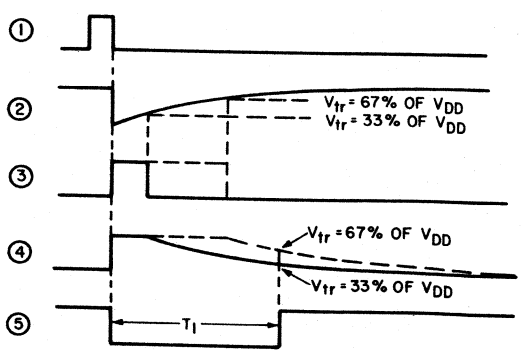


Fig. 89 — Cancelling effects of transfer-voltage variations of two COS/MOS inverters when two equal time constants are used.

than 9 per cent. The total time for one period T1 is approximately 1.4 times the R1C1 time constant.

Unlike the astable circuit, which shows no variation in frequency over the temperature range from −55°C to +125°C, the monostable multivibrator shows some change in time period T. The variation is less than 10 per cent. Table XVI shows data measured on five units over the temperature range. At 25°C, the variation in the time period from unit to unit is quite small, usually less than 5 per cent at a V_{DD} of 10 volts.

The output from inverter B in Fig. 87 can be held in the low or "0" state as long as the R2C2 time constant is recharged by another triggering pulse before the discharge waveform it generates passes through the transfer voltage of inverter B. Diode D2 in Fig. 87 is internal to the COS/MOS circuit. As discussed for the astable oscillator, it is part of the input protection circuit shown in Fig. 80, and serves to clamp the input at V_{DD}.

Table XVI — Frequency variations of monostable multivibrators at three temperatures

Unit No.	Period @ V_{DD} = 10V (ms)		
	-55°C	+25°C	+125°C
2	1.06	1.08	1.00
6	1.015	1.03	0.99
11	1.00	1.02	0.98
13	1.01	1.03	0.97
20	1.02	1.02	0.99

$R_1 = R_2$ = 1 megohm, $C_1 = C_2$ = 0.001μF

Figs. 90 and 91 show two variations of the monostable circuit to-

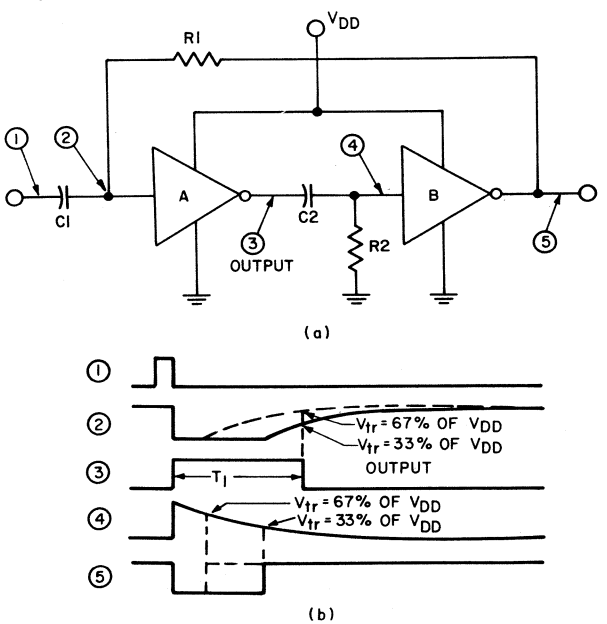


Fig. 90 — (a) Monostable multivibrator triggered by negative-going input pulse; (b) circuit waveforms.

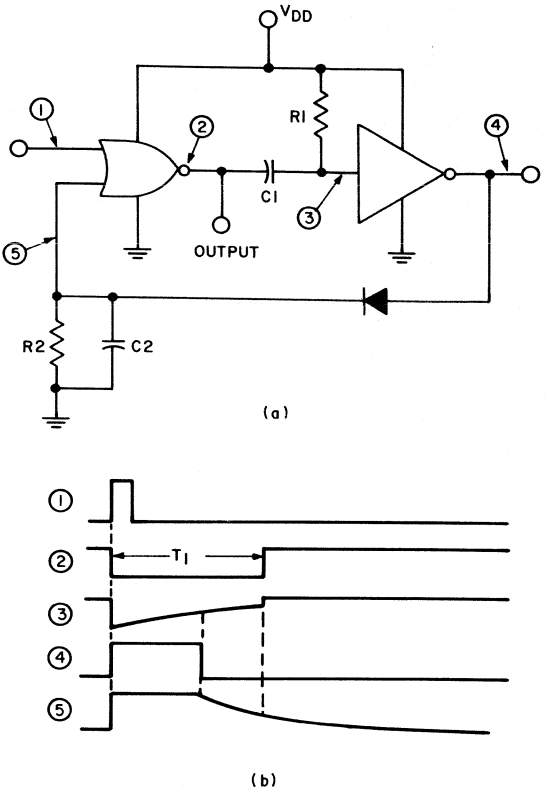


Fig. 91 – (a) Monostable multivibrator triggered by positive-going input pulse; (b) circuit waveforms.

gether with their associated waveforms. The circuit of Fig. 90 triggers on the negative-going excursions of the input pulse, in the same manner as the circuit of Fig. 87. The output pulse is positive-going and is taken from the first inverter. This circuit does not need an external diode. The circuit of Fig. 91 triggers on the positive-going excursion of the input pulse, and then locks back on itself until the RC time constants complete their discharge. The circuits of Figs. 90 and 91 cannot be retriggered until they return to their quiescent states.

Low-Power Circuit

The monostable circuits discussed thus far dissipate some power because one or both of the inverters are ON during the charging or discharging of the RC time constants. This power dissipation will be extremely low provided the one-shot pulse width is short compared to the over-all cycle time. Fig. 92 shows the current waveform associated with the circuit of Fig. 87. This waveform is quite wide at the base, and some current flows for

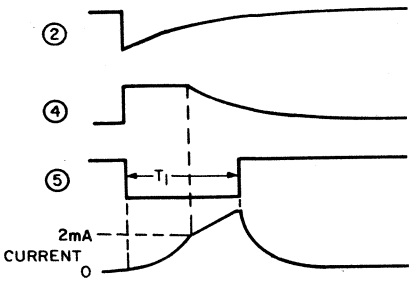


Fig. 92 – Current waveforms for the diode-compensated multivibrator of Fig. 87.

approximately twice the time period. Fig. 93(a) shows a circuit using the CD4007A which dissipates much less power than the other circuits shown, but does not have the same stability. This circuit operates as shown by the waveforms in Fig. 93(b). In the quiescent state, the p-channel transistor of the first inverter is biased OFF while the n-channel transistor (which derives its control from the output of the second inverter) is biased ON. Therefore, the output at C is low, and that at D is high. When a negative-going pulse is introduced into the circuit through capacitor C1, the R1C1 time constant becomes negatively charged, and the p-channel device is turned on. Capacitor C2 then charges to V_{DD}, the output at D becomes low, and the n-channel device of the first inverter is turned off. Capacitor C1 immediately begins to charge to V_{DD} through R1 [waveform (B)]. The p-channel transistor remains ON, keeping capacitor C2 charged to V_{DD}, until the waveform generated passes through its threshold-voltage level and turns it off. The n-channel transistor of the first inverter is still OFF because the output of the second inverter [waveform (D)] is still low. When the p-channel device of the first inverter turns off, capacitor C2 begins to discharge through resistor R2 [waveform (C)] to ground. As it discharges, it passes through the threshold voltage of the second p-channel transistor so that it begins to turn on. The voltage waveform at (D) then begins to rise, and the n-channel device of the first inverter turns on and provides a second discharge path for the capacitor C2. As a result, the output waveform changes state from low to high quite rapidly to complete the cycle.

The major advantage of the circuit of Fig. 93 is its low power dissipation. Because the circuit depends on the p-channel-transistor threshold, the time period T varies from unit to unit or with temperature variations. Some compensation can be provided if the R2C2 time constant is made approximately 3 times larger than the R1C1 time constant, as shown in Table XVII. For minimum current in the circuit of Fig. 93, capacitor C2 can be

Table XVII – Frequency variations of monostable multivibrator with temperature when R_2C_2 time constant is increased

	Period with V_{DD} = 10V (μs)		
Unit No.	-55°C	+25°C	+125°C
553	1090	1120	1160
554	1060	1090	1120
810	1030	1030	1020
900	1000	1020	990
939	1080	1100	1050

R_1 = 0.35 megohm, C_1 = 0.001μF
R_2 = 1 megohm, C_2 = 0.001μF
R_2C_2 is approximately $3R_1C_1$

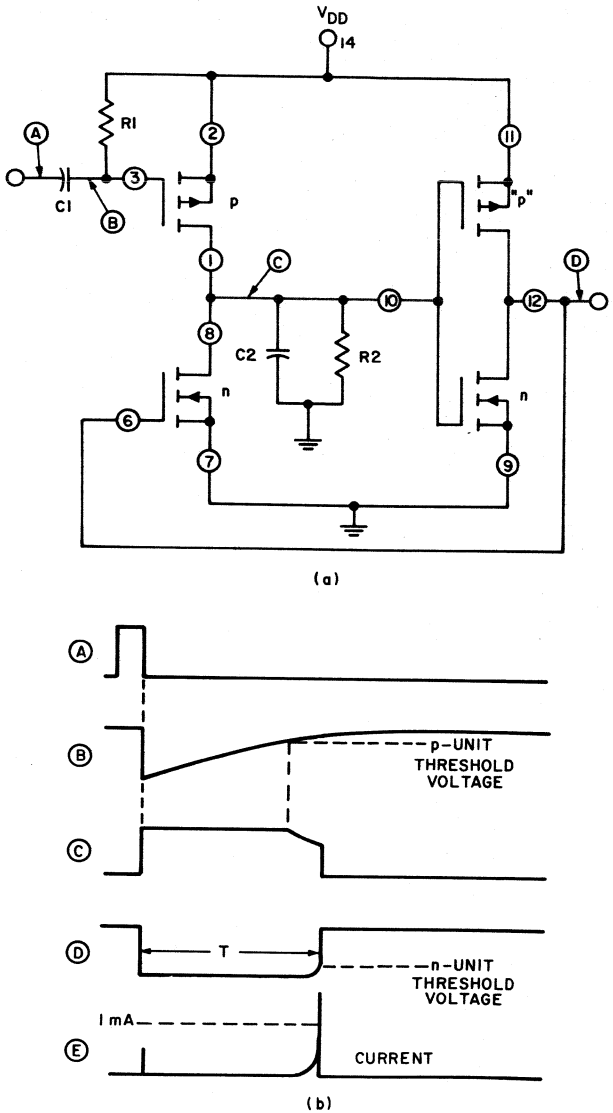


Fig. 93 – (a) Low-power monostable multivibrator using the CD4007A; (b) circuit waveforms.

removed so that only stray capacitance is present at the input of the second inverter. A comparison of time-period variations under this condition is shown in Table XVIII. Again, the variations from unit to unit are caused by differences in p-channel transistor threshold.

Table XVIII — Frequency variations of monostable multivibrator with temperature when C_2 consists of stray capacitance only

Unit No.	Period with V_{DD} = 10V (μs)		
	-55°C	+25°C	+125°C
553	870	940	1020
554	900	970	1050
810	900	1000	1080
900	810	880	960
939	780	850	920

R_1 = 0.62 megohm, C_1 = 0.001μF
R_2 = 1 megohm, C_2 = strays

APPLICATIONS

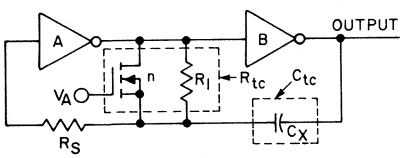
COS/MOS multivibrators can be used in a variety of applications including voltage-controlled oscillators, voltage-controlled pulse-width circuits, phase-locked voltage-controlled oscillators, frequency multipliers, and envelope detectors. Fig. 94(a) shows a voltage-controlled oscillator, a circuit similar to that of Fig. 81(a). (Inverters and n-channel device are available in a single COS/MOS package as the CD4007A.) C_{tc} is variable (by adjustment of C_X) as is R_{tc} (by adjustment of V_A). The value of R_{tc} varies from approximately 1 to 10 kilohms. These limits are determined by the parallel combination of R1 (10 kilohms) and the n-channel resistance which varies from 1 kilohm (R_{ON}) to approximately 10^{11} ohms (R_{OFF}). When V_A and V_{SS} are equal, the n-channel device is OFF, and

$$R_{tc} = \frac{R_{OFF}}{R_1} \approx R1 = 10 \text{ kilohms} \quad (16)$$

because R_{OFF} is much greater than R1. When V_A and V_{DD} are equal, the n-channel device is fully ON, and

$$R_{tc} = \frac{R_{ON}}{R_1} \approx R_{ON} = 1 \text{ kilohm} \quad (17)$$

because R_{ON} is very much less than R1. The oscillator center frequency is varied by adjustment of C_X. Fig. 94(b) shows a comparison of the period of the output waveform as a function of V_{DD} and V_A.



TYPICAL VALUES
R_1 = 10,000 OHMS C_X = 0.001 TO 0.004 μF
R_S = 100,000 OHMS $0 \le V_A \le V_{DD}$

PERIOD OF OUTPUT (MICROSECONDS) AS A FUNCTION OF V_A AND V_{DD}

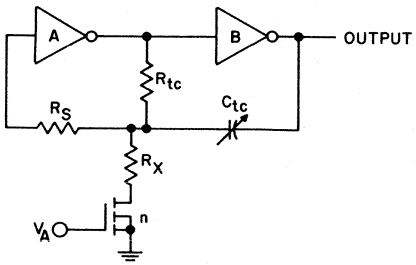
V_A (VOLTS)	V_{DD} (VOLTS)		
	5	10	15
0	120	54	48
5	115	45	41
10	—	32	30
15	—	—	24

(b)

Fig. 94 — (a) Voltage-controlled oscillator using one CD4007A; (b) period of outputs as a function of V_A and V_{DD}.

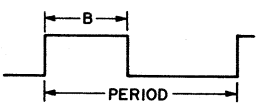
Voltage-Controlled Pulse-Width Circuit

Fig. 95(a) shows a further modification of the circuit of Fig.81(a) which causes the pulse width to be modulated, by varying V_A, only when R_X is sufficiently high. For example, if C is 0.0022 microfarad, then R_X is approximately 35 kilohms. Lower values of R_X affect the frequency of oscillation. If R_X is less than 10 kilohms, there is a value of V_A which will



TYPICAL VALUES
R_{tc} = 10,000 OHMS
R_S = 100,000 OHMS
R_X = 35,000 OHMS
C_{tc} = 0.0005 TO 0.0025 μF

(a)



PULSE WIDTH B(MICROSECONDS)
AS A FUNCTION OF V_A AND V_{DD}

V_A (VOLTS)	V_{DD} (VOLTS) PERIOD (MICROSECONDS) 5V 41.5μS	10V 35μS	15V 33μS
	PULSEWIDTH (MICROSECONDS)		
0	23	19.3	17
5	20	17.7	16.2
10	—	16.2	15.5
15	—	—	14.3

C_{tc} = 0.0015 μF

(b)

Fig. 95 — (a) Voltage-controlled pulse-width circuit; (b) period and pulse width of output as a function of V_A and V_{DD}.

cause the oscillator to cut off. Fig. 95(b) shows the output waveform and values of pulse width (B) for various values of V_A and V_{DD}.

Phase-Locked Voltage-Controlled Oscillator

The voltage-controlled oscillator (VCO) can be operated as a phase-locked oscillator by the application of a frequency-controlled voltage to the gate of the n-channel device. Fig. 96 shows the block diagram of an FM discriminator using the phase-locked VCO. The first block is the

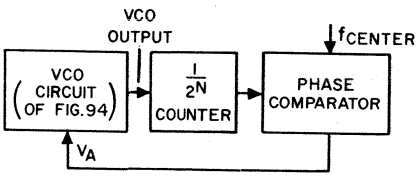
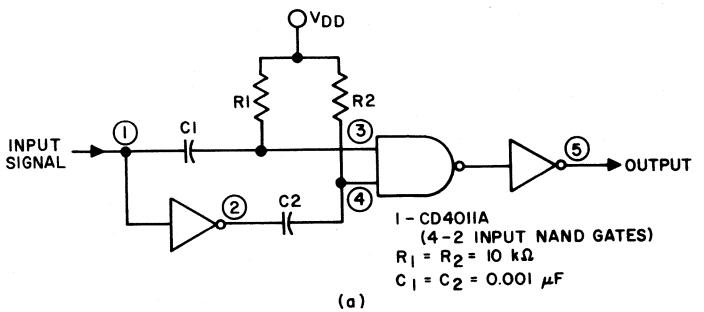


Fig. 96 — FM discriminator using the phase-locked voltage-controlled oscillator

same circuit as that shown in Fig. 94. When the two inputs to the phase comparator are different, the comparator produces an output which is fed to the gate of the n-channel device (V_A). The change of V_A causes the output frequency of the VCO to change. This change is divided by 2^N and fed back to the phase comparator.

Frequency Multipliers

Fig. 97(a) shows a frequency doubler. A 2^N multiplier can be realized by cascading this circuit with N − 1 other identical circuits. The leading edge of the input signal is differentiated by R1 and C1 and applied to input (a) of the NAND gate. This action produces a pulse at the output. The trailing edge of the input pulse, after being inverted, is differentiated and applied to input (b) of the NAND gate. This action produces the second output pulse from the NAND gate. The waveforms for 5 points in the circuit are shown in Fig. 97(b).



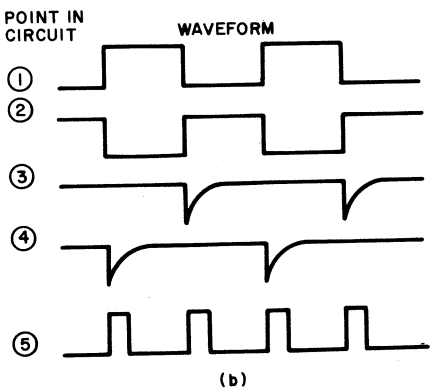


Fig. 97 – (a) Frequency-doubler circuit using one CD4011A; (b) circuit waveforms.

Modulation/Demodulation-Envelope Detection

Pulse modulation is accomplished by use of the circuit shown in Fig. 98(a), a variation of the circuit of Fig. 81(a). The oscillator is gated ON or OFF by the signal impressed at input (1) of the NAND gate. Waveforms for the pulse-modulation circuit are shown in Fig. 98(b).

Demodulation or envelope detection of pulse-modulated waves is performed by the circuit shown in Fig. 99(a). The carrier burst is inverted by inverter A. Its first negative transition at point (2) turns

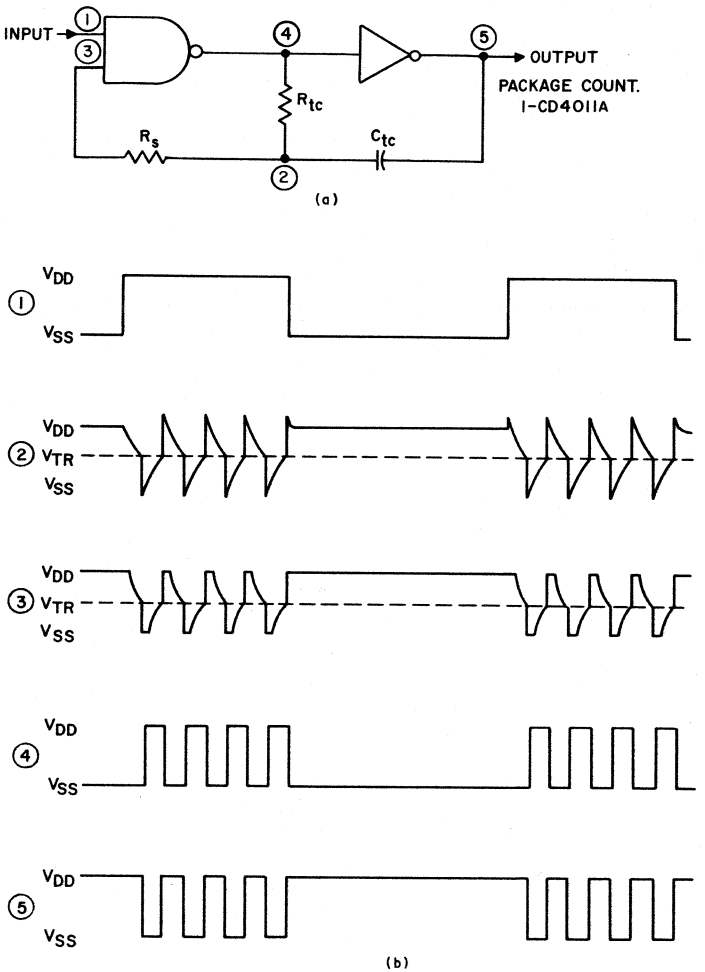


Fig. 98 – (a) Modulator circuit using one CD4011A; (b) circuit waveforms.

on diode D and provides a charging path for C_{tc} through the n-channel resistance to ground. On the positive transition of the signal at point (2), the diode is cut off, and C_{tc} discharges through R_{tc}. The discharge time constant ($R_{tc}C_{tc}$) is much greater than the time of the burst duration. Point (3), therefore, never displays the conditions required for the switching of inverter B until the burst has passed. The waveforms for 4 points in the circuit are shown in Fig. 99(b).

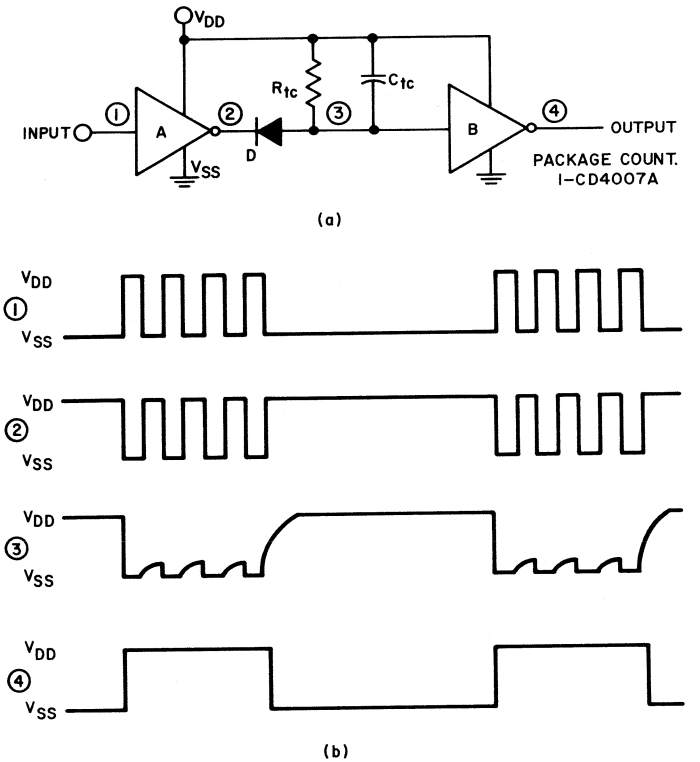


Fig. 99 – (a) Demodulator (envelope-detector) circuit using one CD4007A; (b) circuit waveforms.

Thirty-Two-Bit Adder

This section describes the design of a COS/MOS arithmetic unit capable of adding, subtracting, multiplying, and dividing as well as performing the logical functions OR, AND, and Exclusive-OR on two 4-bit words. Three 4-bit registers permit either of two words to perform the desired operation with the third. The unit consists of COS/MOS devices including registers, AND-OR select gates, a full adder, and NOR and NAND logic gates.

FUNCTIONAL DESCRIPTION OF ARITHMETIC UNIT

A block diagram of the 4-bit arithmetic unit is shown in Fig. 100. The required package count and the function performed by each package are shown in Table XIX. A brief description of each of the COS/MOS devices used to configure the arithmetic unit is given below.

Four-Bit Full Adder (CD4008A)

The CD4008A consists of four full-adder stages with fast look-ahead carry provision from stage to stage. The logic diagram for this device is shown in Fig. 101. Circuitry is included to provide a fast parallel-carry-out bit to permit high-speed operation in arithmetic sections that use several CD4008A's.

The CD4008A inputs include the four sets of bits to be added, A_1 to A_4 and B_1 to B_4, in addition to the carry-in bit from a previous section. CD4008A outputs include the four sum bits, S_1 to S_4, in addition to the high-speed parallel-carry-out, which may be used at a succeeding CD4008A section.

Quad AND-OR Select Gate (CD4019A)

The CD4019A, as shown in the logic diagram in Fig. 102, consists of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to simple selection of either channel A or channel B information, the control bits can be applied in combination to accomplish a third selection of data.

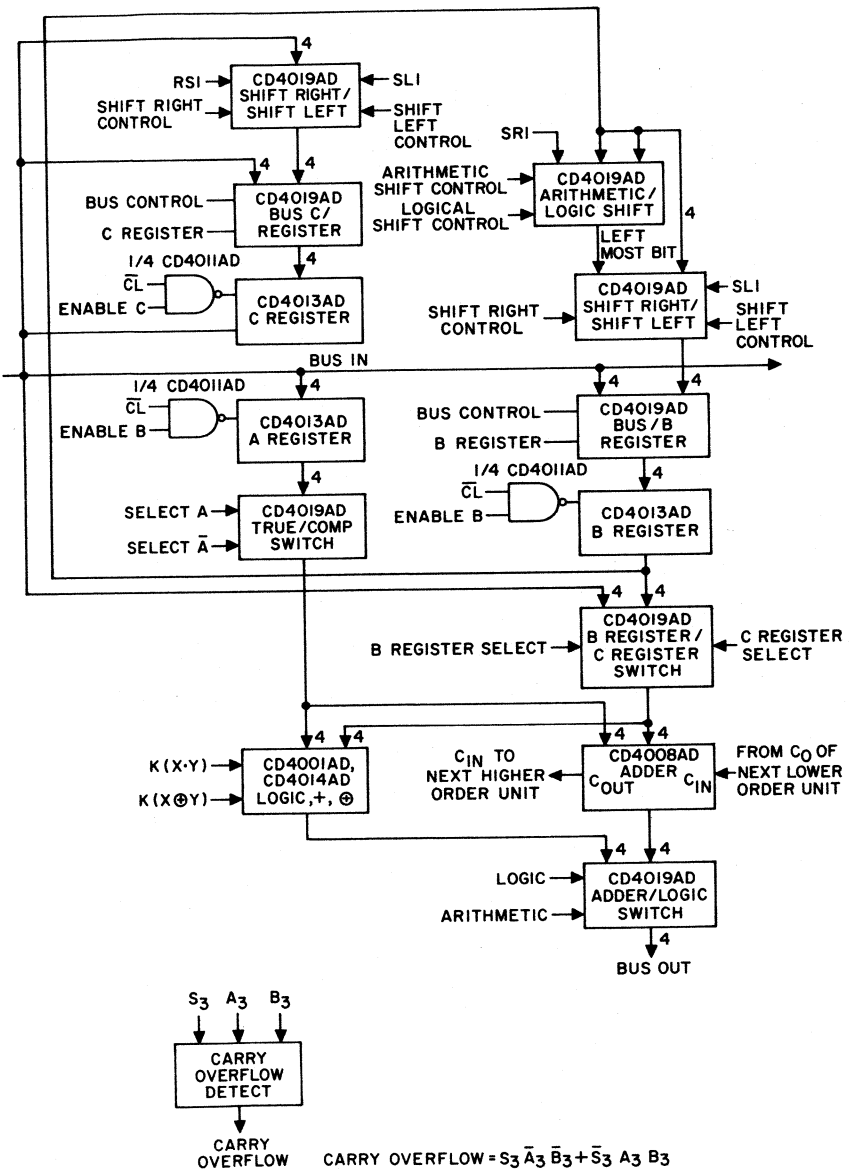


Fig. 100 — Block diagram of the 4-bit arithmetic unit.

Table XIX — Function and Package Count of Devices in Arithmetic Unit

Function	Packages				
	CD4008A	CD4019A	CD4013A	CD4011A	CD4001A
A Register (includes A, $\overline{A}$ select capability and buffered outputs)		1	2		
B Register (includes shift capability and buffered outputs for B and $\overline{B}$)		3	2		
C Register (includes shift capability and buffered outputs)		2	2		
Select B or C		1			
Add	1				
Perform logic		1			5
Select logic or addition		1			
Overflow detector					1
Clock inhibit				1	
Total	1	9	6	1	6

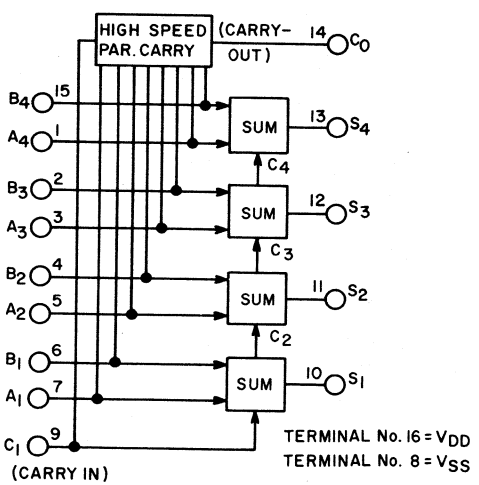
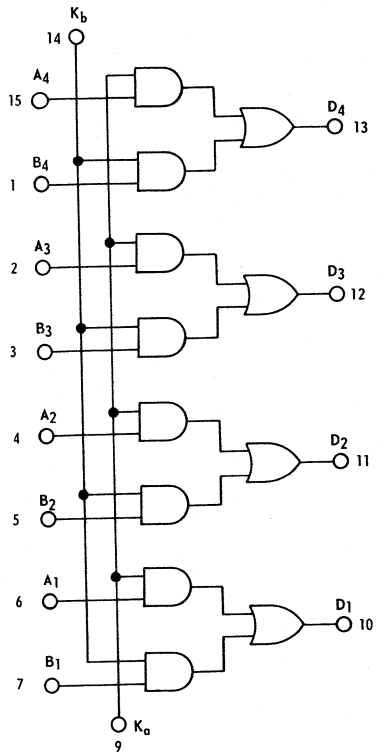


Fig. 101 — CD4008A 4-bit full adder.



TYPICAL EQUATION AND TRUTH TABLE FOR 1 OF 4 SELECT GATES (POSITIVE LOGIC "1" = V_{DD}; "0" = GND)

$D_1 = (A_1 \cdot K_a) + (B_1 \cdot K_b)$

K_a	K_b	D
0	0	0
1	0	A
0	1	B
1	1	A+B

8 = GND
16 = V_{DD}

Fig. 102 – CD4019A quad AND-OR select gate.

Dual D-Type Flip-Flop (CD4013A)

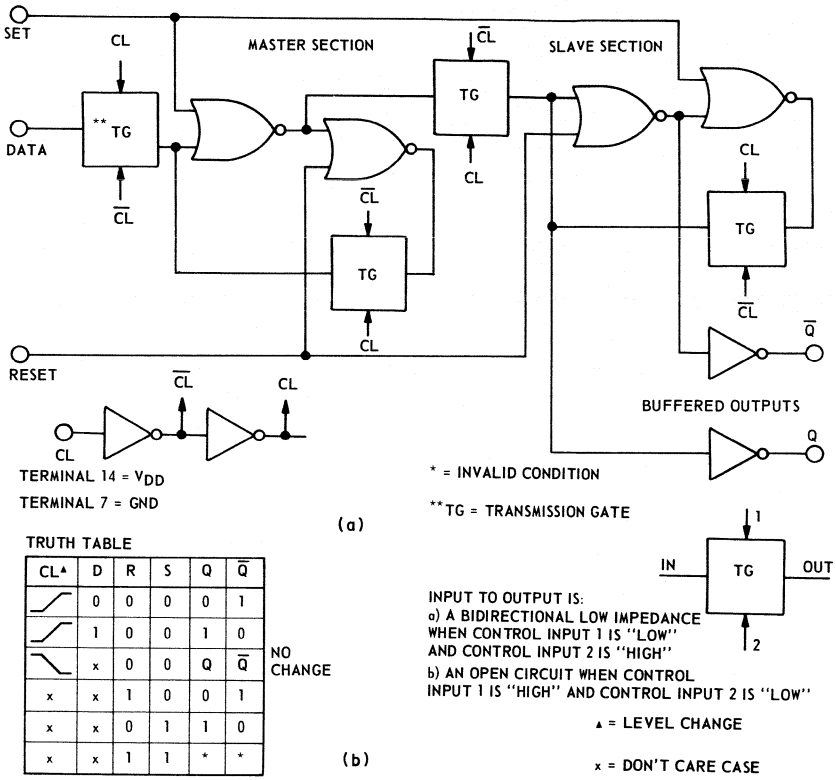
The CD4013A consists of two identical independent data-type flip-flops on a single monolithic silicon chip; the logic diagram for one flip-flop is shown in Fig. 103. Each flip-flop has independent data, reset, set, and clock inputs and complementary buffered outputs. The CD4013A can be used in shift-register applications and for counter and toggle applications by connecting the Q output to the data input. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Resetting or setting is accomplished by a high level on the reset or set line, respectively.

NAND Gates (CD4011A)

The CD4011A consists of four identical independent 2-input positive-logic NAND gates. Fig. 104 shows the logic diagram and equations for this device.

NOR Gates (CD4001A)

The CD4001A consists of four identical independent 2-input positive-logic NOR gates. Fig. 105



TRUTH TABLE

CL▲	D	R	S	Q	$\overline{Q}$	
⌐⌐	0	0	0	0	1	
⌐⌐	1	0	0	1	0	
⌐_	x	0	0	Q	$\overline{Q}$	NO CHANGE
x	x	1	0	0	1	
x	x	0	1	1	0	
x	x	1	1	*	*	

(b)

Fig. 103 — (a) One of two identical flip-flops composing the CD4013A dual D-type flip-flop; (b) circuit truth table.

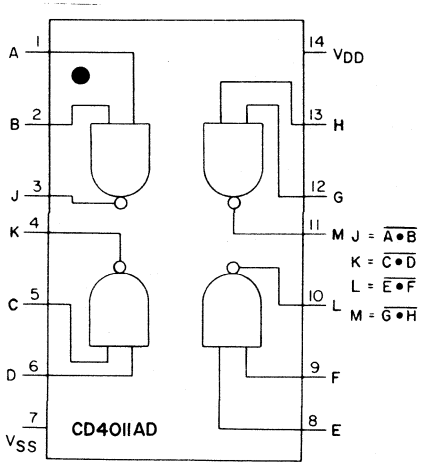


Fig. 104 — CD4011A NAND gate.

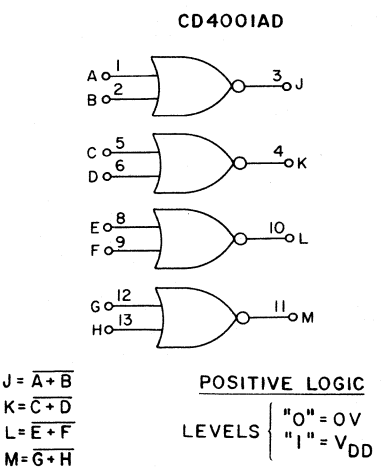


Fig. 105 — CD4001A NOR gate.

Table XX – Terms and Symbols Used in Arithmetic Unit Drawings

Symbol	Function
IN_0	Lowest-order bus input
IN_1	Second-lowest-order bus input
IN_2	Third-lowest-order bus input
IN_3	Highest-order bus input
$\overline{Inh_1}$	Inhibits A register
$\overline{Inh_2}$	Inhibits B register
$\overline{Inh_3}$	Inhibits C register
A	Selects true of A-register data for half output function
$\overline{A}$	Selects complement of A-register data for half output function
SEL B	Selects B-register data for output function with A-register data
SEL C	Selects C-register data for output function with A-register data
Arithmetic Shift	Allows B register to shift in the arithmetic mode
Logic Shift	Allows C register to shift in the logical mode
B Bus	Allows B register to accept data from bus inputs
B Shift	Allows B register to shift right or left
B SR	Allows B register to shift right
B SL	Allows B register to shift left
B SRI	Input to lowest-order bit of B register when shifting right
B SLI	Input to highest-order bit of B register when shifting left
C Bus	Allows C register to accept data from bus inputs
C Shift	Allows C register to shift right or left
C SR	Allows C register to shift right
C SL	Allows C register to shift left
C SRI	Input to lowest-order bit of C register when shifting right
C SLI	Input to highest-order bit of C register when shifting left
Arithmetic	Allows logical sums to appear at S outputs
Logic	Allows logic functions to appear at S outputs
C_{in}	Carry in to lowest-order bit of adder
C_{out}	Carry out from highest-order bit of adder
Overflow	Indicates if addition exceeds limit of adder
K[·]	Generates logical AND of logic circuits
K [⊕]	Generates logical Exclusive - OR of logic circuits
S_0	Lowest-order output
S_1	Second-lowest-order output
S_2	Third-lowest-order output
S_3	Highest-order output (sign bit)

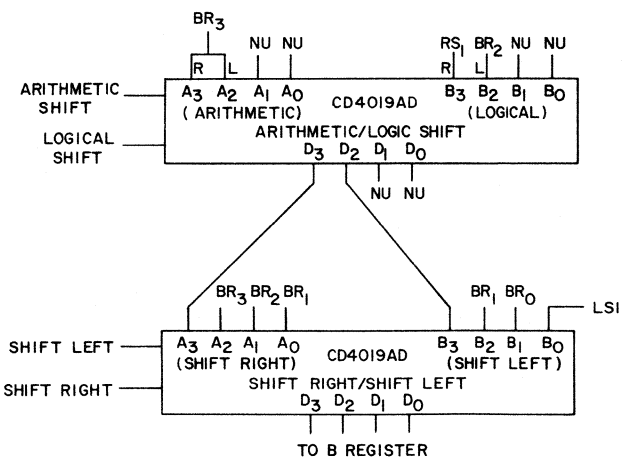
shows the logic diagram and equations for this device.

ARITHMETIC-UNIT OPERATION

The circuit elements included in the arithmetic unit are shown in Fig. 100; the terms and symbols used are defined in Table XX. The A register uses a CD4019A quad AND-OR select gate to present either the true or complemented data to the logic circuits and the adder. Thus, the data in the A register can be either added to or subtracted from the B or C registers.

The CD4019A at the input of the B register has two control lines to permit data to be shifted right or left, or to permit new data to be accepted from the bus lines. A detailed interconnection diagram of the shift-right/shift-left and arithmetic/logic-shift circuit is shown in Fig. 106. The arithmetic-shift mode is used only on the highest-order bits and assures that the sign bit does not change during shifting. On the lowest-order bits, the left-shift input for the B register (BLSI) is set to zero. On all other stages, the BLSI is tied to the B_3 output of the next lower set of bits.

The C register is identical to the B register but provides only for logical shifting. Separate shift-right and shift-left controls are provided for the B and C registers (BSL and BSR for the B register, and CSL and CSR for the C register). Another CD4019A is used to select either B or C register information for the logic or arithmetic operations.



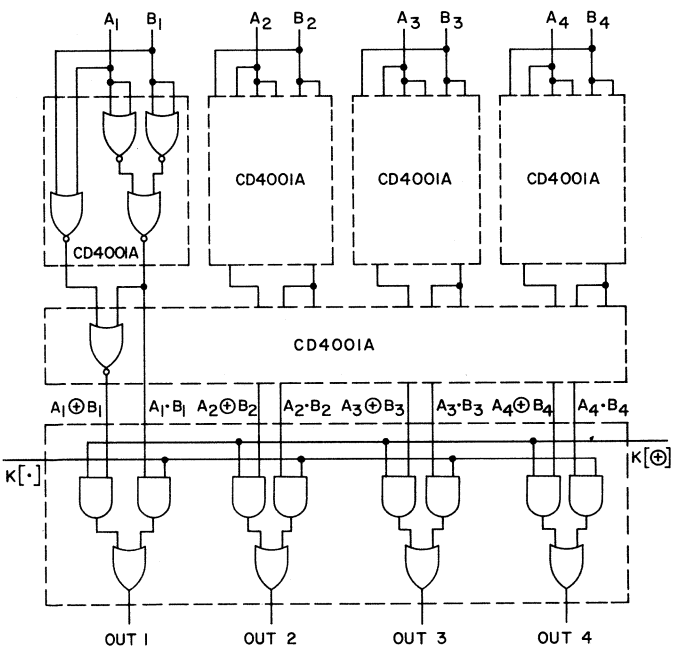
RSI = RIGHT SERIAL INPUT
LSI = LEFT SERIAL INPUT
BR_n = OUTPUT OF n^{th} BIT OF "B" REGISTER
NU = NOT USED

Fig. 106 — Interconnection diagram, shift right/shift left-arithmetic/logic shift.

The logic diagram for the AND/OR/Exclusive-OR logic selector is shown in detail in Fig. 107; 1¼-CD4001A's and ¼-CD4019A are used per bit (or 5-CD4001A's and 1-CD4019A per four-bit word). The control inputs are labeled K [·] (K-AND) and K [⊕] (K-Exclusive OR). If B_1 is an output from the B register and A_1 is a true output from the A register through the True/Complement Switch shown in Fig. 100, then logic selection operates as follows:

When K[·] is high and K[⊕] low, the logic generated is A ·B. When K [·] is low and K [⊕] high, the logic generated is A $\veebar$ B = AB + AB. When both K [·] and K [⊕] are high, the logic is AB + $A\veebar B$ = AB + AB + AB = A + B.

The adder is a single CD4008A whose carry input is tied to the carry output of the adder on the next-lower-order CD4008A. The carry input of the lowest-order bits is 0 for addition and 1 for 2's-complement subtraction. The output buffer is



TRUTH TABLE

K[·]	K[⊕]	OUT
0	0	0
1	0	A·B
0	1	A⊕B
1	1	A+B

Fig. 107 — AND/OR/Exclusive-OR logic selector.

another CD4019A. In this application, this device is used to select either arithmetic or logic outputs and to provide more output drive.

The output of the overflow logic circuit shown in Fig. 108 goes high if the adder result exceeds the total bit capacity of the arithmetic unit. This overflow occurs only when two numbers having the same sign bit are added and the result is a sum having the opposite sign.

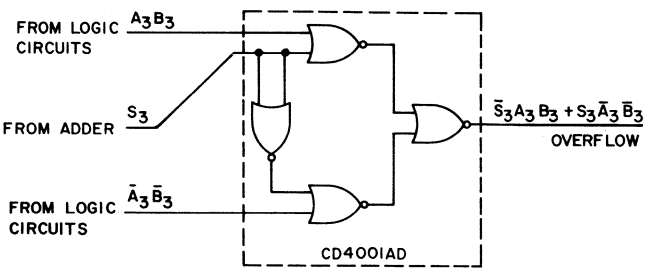


Fig. 108 — Overflow logic circuit.

The arithmetic unit can be made to operate on words of any desired length by cascading additional circuits. The interconnection of eight of the units shown in Fig. 100 to form a 32-bit arithmetic unit is shown in Fig. 109. The three inhibit signals, common control signals, and clock-not signal, all of which are common to all eight sub-units, are not shown.

PERFORMANCE DATA

In a 32-bit arithmetic unit constructed in the laboratory, the delay time under worst-case conditions for the clock-not to be inverted, for data to be written into the register, and for that data to get to the adder and generate a carry-out from a 4-bit unit was 782 nanoseconds. The delay time under worst-case logic conditions for a carry-in to generate a carry-out was 87 nanoseconds. The delay time under worst-case logic conditions for a carry-in to generate a sum at the adder and for this sum to appear at the output was 623 nanoseconds. These numbers result in an addition time of 1927 nanoseconds (782 + 6 x 87 + 623) for two 32-bit words and 1579 nanoseconds (782 + 2 x 87 + 623) for two 16-bit words.

Since the construction of the adder used to collect the above data, improved processing techniques have increased its potential for faster operation. It is now possible to achieve delays from clock to carry-out of less than 500 nanoseconds, delays from carry-in to carry-out of less than 50 nanoseconds, and delays from carry-in to sum-out of less than 400 nanoseconds. Thus, the worst-

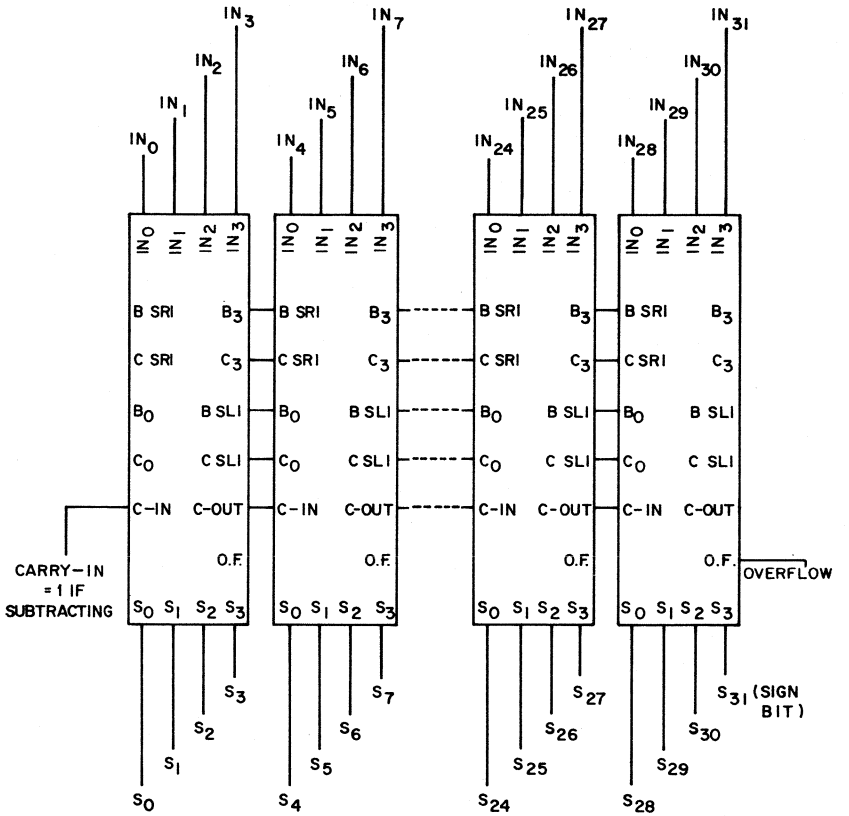


Fig. 109 – Interconnection of eight 4-bit arithmetic units of Fig. 100 to form a 32-bit unit.

case addition time is approximately 1200 nanoseconds for a 32-bit arithmetic unit and 1000 nanoseconds for a 16-bit unit.

Calculations based on typical and maximum device quiescent-power dissipation at a 10-volt supply and a +25°C temperature indicate a typical dissipation of 100 microwatts and a maximum dissipation of 2350 microwatts for a 4-bit arithmetic unit.

Counters and Registers

This section shows logic and schematic diagrams for each of the counter and register types available, outlines circuit designs, and discusses device-design tradeoffs. Performance criteria are summarized, and applications by type are described by means of logic or subsystems diagrams and waveforms. Possible extensions of design into other areas of application are given. Counters and registers presently available include the following.

CD4006A—Eighteen-Stage Static Shift Register
CD4014A—Eight-Stage Synchronous Parallel-Input/Serial-Output Register
CD4015A—Dual Four-Stage Serial-Input/Parallel Output Register
CD4017A—Decade Counter and 10 Decimal Decoded Outputs
CD4018A—Presettable Divide-by N Counter
CD4020A—Fourteen-Stage Binary Counter
CD4021A—Eight-Stage Asynchronous Parallel-Input/Serial Output Register
CD4022A—Divide-by-8 Counter and 10 Decimal Decoded Out-Outputs
CD4024A—Seven-Stage Binary Counter with Buffered Reset
CD4026A—Decade Counter/Divider with Seven-Segment Display Outputs and Display Enable
CD4029A—Presettable Up/Down Counter
CD4033A—Decade Counter/Divider with Seven-Segment Display Outputs and Ripple Blanking

The applications shown also utilize other COS/MOS family types, such as the CD4000A, CD4001A, and CD4002A NOR gates; CD4013A dual-D flip-flop; CD4007A dual complementary pair plus inverter; CD4009A and CD4010A hex/buffer/logic-level converters; and the

CD4011A and CD4012A quad-2 and dual-4 NAND gates.

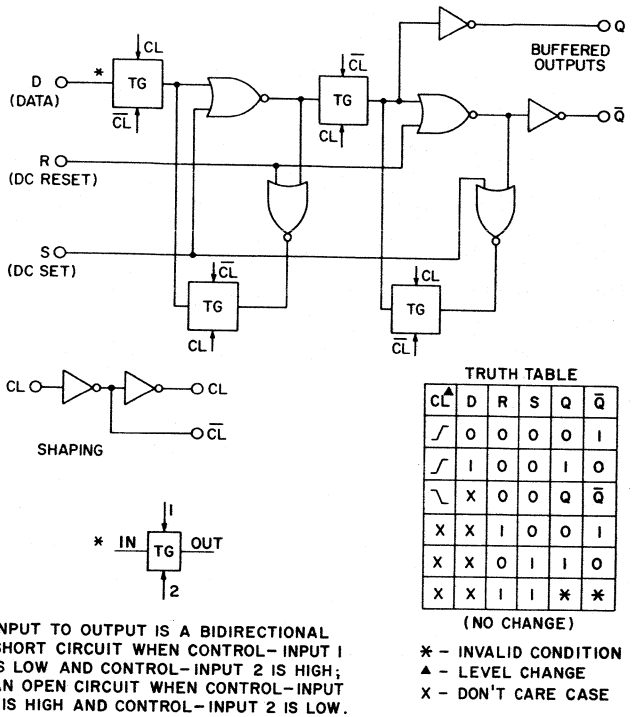
CIRCUIT DESIGN

COS/MOS counters and registers consist of between 100 and 300 MOS devices, supporting interconnect tunnels, metal runs, and bond pads, all on a single monolithic pellet. Table XXI summarizes the major operating characteristics of the counters and registers. Not all possible applications are shown in this section; those shown highlight typical counter and register uses.

Fig. 110 illustrates the basic static master-slave flip-flop circuit configuration utilized in all COS/MOS counters and registers. The logic level present at the D (data) input is transferred to the Q output

Table XXI — Typical Features and Characteristics of COS/MOS Counters and Registers

Features		
Operating-Temperature Range	-55 to +125°C (Ceramic Package) -40 to +85°C (Plastic Package)	
Operating-Voltage Range (V)	3 to 15	
Full MOS Gate-Oxide Protection at all Terminals.		
Output Buffers Provided		
Full Static Operation		
Characteristics (T_A = +25°C)	**V_{DD} = 10 Volts**	**V_{DD} = 5 Volts**
Clock-Pulse Frequency (MHz)	5	2.5
Clock Rise and Fall Times (μs)	5	5
Quiescent Power Dissipation per Package (μW)	5	1.5
Noise Immunity — All Inputs	45% of V_{DD}	
Drive Capability	I_D = 0.5 to 3 mA @ V_1 = 7 V	I_D = 0.1 to 1 mA @ V_1 = 4 V
Sink Capability	I_D = 0.5 to 3 mA @ V_0 = 3 V	I_D = 0.1 to 1 mA @ V_0 = 1 V



$C\overline{L}$	D	R	S	Q	$\overline{Q}$
∫	0	0	0	0	1
∫	1	0	0	1	0
⌝	X	0	0	Q	$\overline{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	*	*

Fig. 110 - Basic COS/MOS master-slave flip-flop stage.

during the positive-going transition of the clock pulse. DC reset or set is accomplished by a high level at the respective input. Both reset and/or set functions are easily omitted as shown in some of the designs. Output lead isolation at the Q and/or $\overline{Q}$ outputs is realized by use of inverters. These inverters eliminate all possibility of MOS gate-oxide damage at the output leads, and also improve circuit speed, noise immunity, and drive capability. The sizes of the p-channel and n-channel MOS devices in the output inverters are tailored to meet the desired drive- and sink-current requirements. The internal clock shaping shown permits a loosely specified input waveshape requirement. As shown in Table XXI, the basic flip-flop configuration operates from a non-critical single-phase clock input signal. Both 1 and 0 clock-pulse durations can go to infinity, and rise and fall times of 5 microseconds or less are permissible.

SEVEN-STAGE RIPPLE-CARRY BINARY COUNTER (CD4024A)

Fig. 111 shows the logic diagram of the CD4024A, a seven-stage ripple-carry binary counter with buffered reset. Fig. 112 and 113 show the schematic and logic dia-

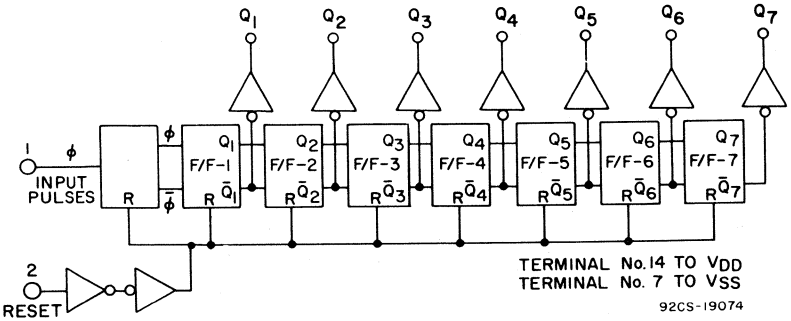


Fig.111 - Logic diagram for CD4024AE 7-stage binary counter with buffered reset.

grams for one of the seven counter stages. Operation is similar to that of the basic master-slave flip-flop, with the following exceptions: The D-line connection is derived from the Q output of that stage so that it complements the stage at the negative clock-pulse transition. The clocking of a stage is derived from the previous counter stage (ripple carry). The dc reset function is realized by raising the ground return path of the

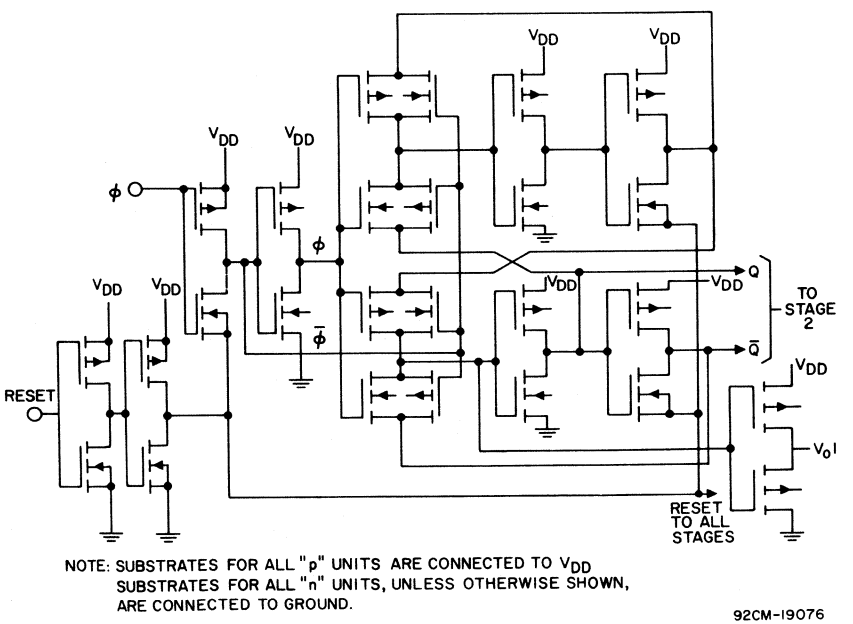
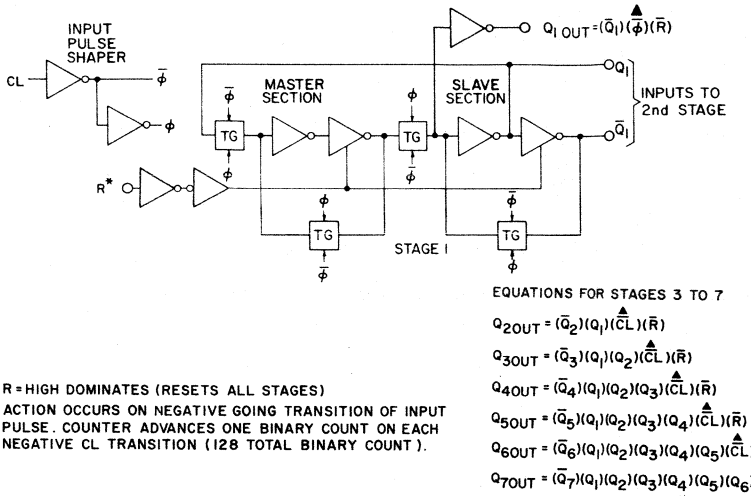


Fig.112 - Schematic diagram for pulse shaper and one binary stage of the CD4024A seven-stage binary counter.



$Q_{1\,OUT} = (\overline{Q}_1)(\blacktriangle\phi)(\overline{R})$

$Q_{2OUT} = (\overline{Q}_2)(Q_1)(\blacktriangle\overline{CL})(\overline{R})$

$Q_{3OUT} = (\overline{Q}_3)(Q_1)(Q_2)(\blacktriangle\overline{CL})(\overline{R})$

$Q_{4OUT} = (\overline{Q}_4)(Q_1)(Q_2)(Q_3)(\blacktriangle\overline{CL})(\overline{R})$

$Q_{5OUT} = (\overline{Q}_5)(Q_1)(Q_2)(Q_3)(Q_4)(\blacktriangle\overline{CL})(\overline{R})$

$Q_{6OUT} = (\overline{Q}_6)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(\blacktriangle\overline{CL})(\overline{R})$

$Q_{7OUT} = (\overline{Q}_7)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(Q_6)(\blacktriangle\overline{CL})(\overline{R})$

Fig.113 - Logic diagram for pulse shaper and one binary stage of the CD4024A seven-stage binary counter.

$\overline{Q}$ outputs of all seven stages (both master and slave sections). This mode of resetting saves four devices and associated interconnections per counter stage. An internal reset driver is provided so that the reset input presents only one COS/MOS load.

Fig. 114 illustrates the use of the CD4024A as a binary frequency

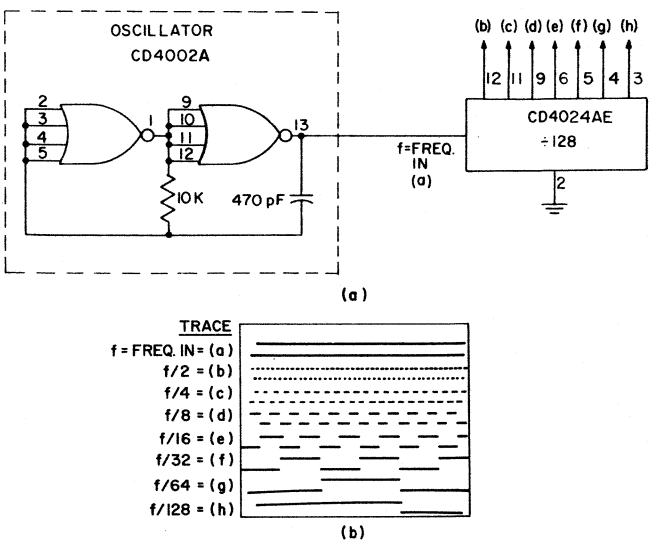


Fig.114 - (a) CD4024AE binary frequency-divider application; (b) circuit waveforms.

divider. Multiple CD4024A units can be stacked for added frequency division. The clock input of a subsequent CD4004A is derived directly from the last output stage of the previous CD4024A. Fig. 115 shows how the CD4024A is used to derive a desired pulse-output delay time. Varied delay times can be realized by detecting different CD4024A outputs. A finer control of delay time is possible if more than one CD4024A output is detected. Extremely long and accurate delay times can be realized by use of an accurate oscillator and multiple CD4024A units.

Figs. 116, 117, and 118 illustrate the use of the CD4024A to derive various divide-by-N counter configurations. Figs. 116 and 117 illustrate two reliable reset methods for counting to the number N (N=60). Reset mode 1 is shown in Fig. 116. The type-D flip-flop is set at the coin-

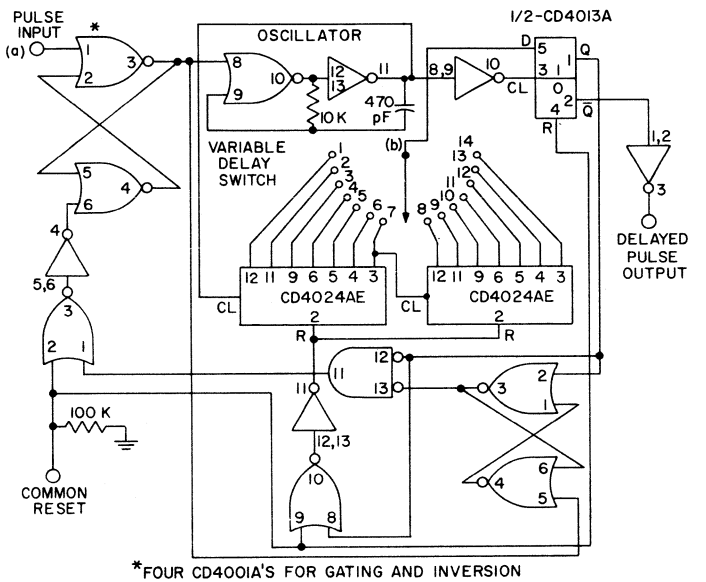


Fig.115 - (a) CD4024AE pulse-delay-control application; (b) circuit waveforms.

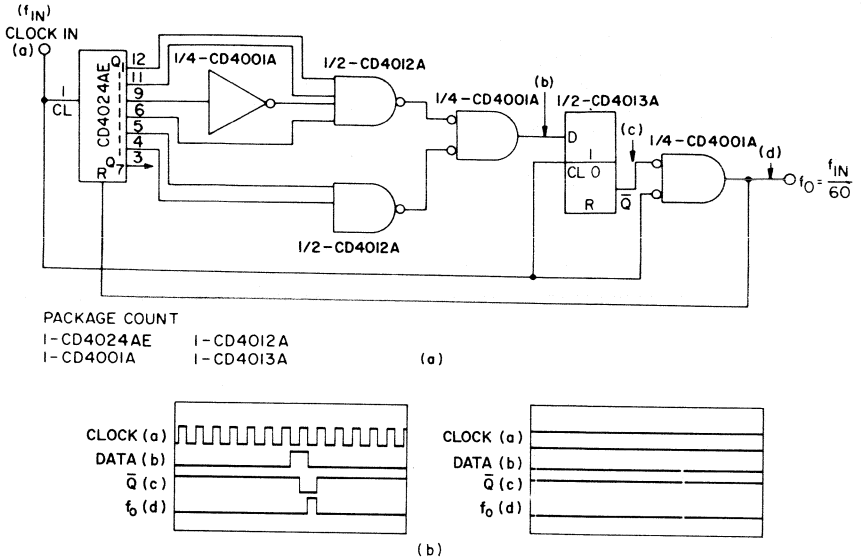


Fig. 116 - (a) Divide-by-60 circuit using the CD4024AE and reset mode 1; (b) circuit waveforms.

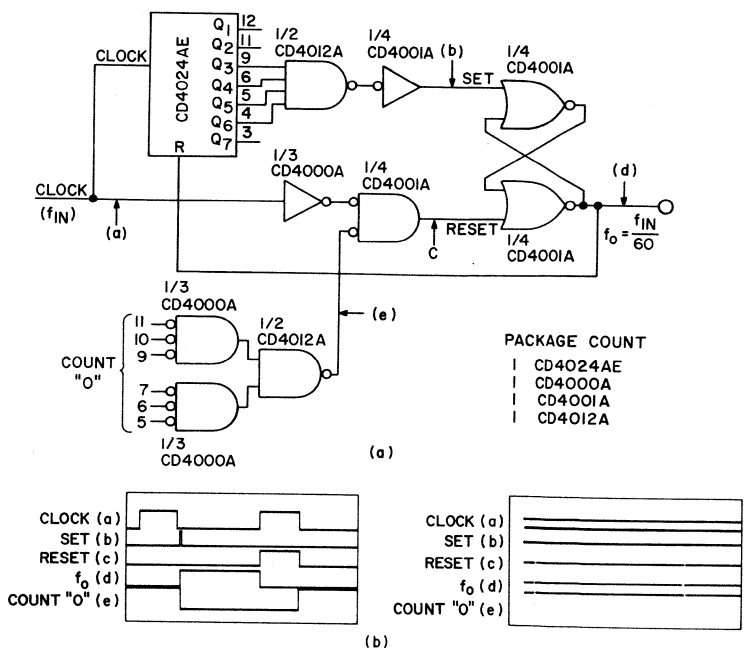


Fig.117 - (a) Divide-by-60 circuit using the CD4024AE and reset mode 2; (b) circuit waveforms.

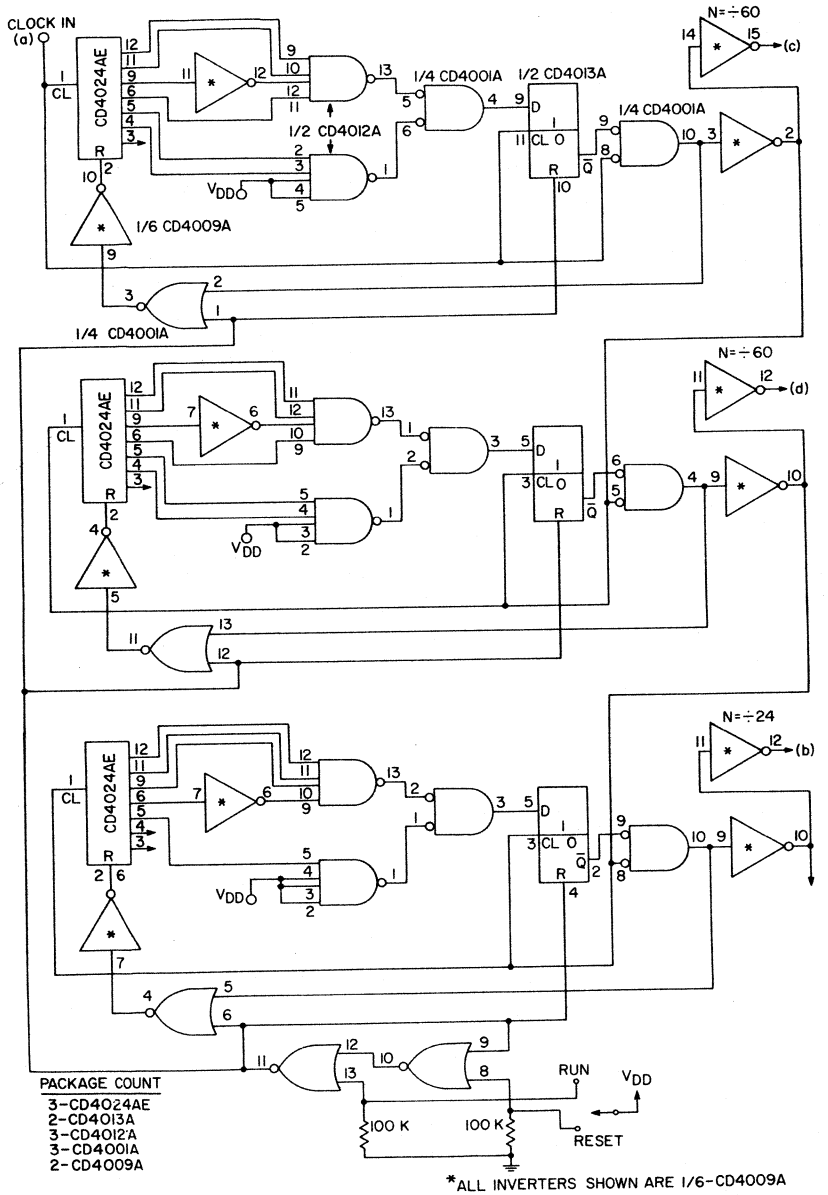
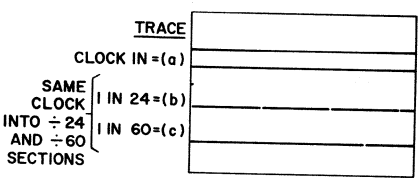


Fig. 118 - Divide-by-60, divide-by-60, and divide-by-24 sections of a CD4024AE divide-by-N counter.

cidence of count 59 and the positive clock transistion. At the next negative clock transition, a reset pulse is generated whose duration is half the clock cycle time. This pulse resets the CD4024A to zero. Only count 59 need be detected for the reset operation; no N + 1 count occurs. Reset mode 2 is shown in Fig. 117. The N + 1 count (60) is detected and sets the R-S (set-reset) flip-flop which, in turn, resets the CD4024A to the zero state. The reset pulse width is half the clock cycle time and is removed by gating count zero with the positive clock transition to reset the R-S flip-flop.

Fig. 118 illustrates a divide-by-60, divide-by-60, divide-by-24 timer using the reset scheme of Fig. 116. Fig. 119 shows the waveforms for this circuit. Similar use of one



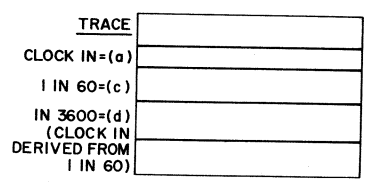
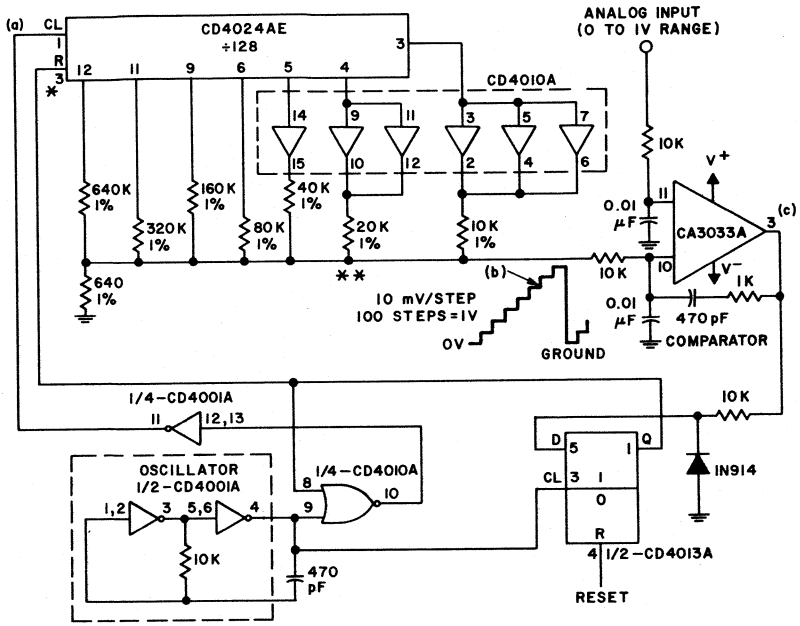


Fig. 119 - Waveforms for counter circuit shown in Fig. 118.

CD4024A unit permits any divide by N from 2 to 128. In applications in which decimal display outputs are required, the CD4017A can be used to advantage, as described below.

Fig. 120 shows how the CD4024A is used with a weighted resistor network to realize analog-to-digital (A-to-D) conversion. The CD4010A (non-inverting hex buffer) is used to reduce the more significant counter output-1-level impedances (which have poor tolerances) to well below the precision-resistor-network values. Varied ranges of analog signals can be handled by control of the resistor network and comparator. As the CD4024A counter advances, the voltage input to the comparator rises until it equals the analog input. The comparator then switches and inhibits further counter advancement, thus holding the digital representation of the analog signal in the counter. Because the CD4024A can count to 2^7, or 128, division of an analog voltage range into 100 parts is easily realized. (The example in Fig. 120 shows a 1-volt range broken into 10-millivolt steps.)

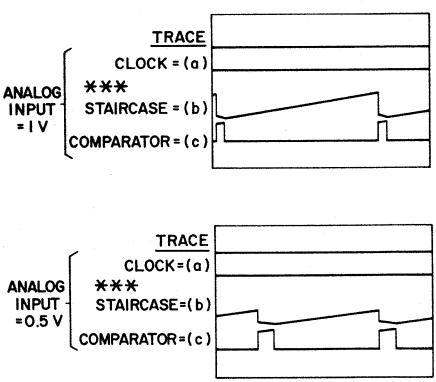
Fig. 121 shows the CD4024A used with an R-2R ladder network for A-to-D conversion. The R-2R network, while requiring added resistors, utilizes only 2 resistor values, permits ready expansion to greater than 7 stages, provides better resistor-temperature tracking, and allows elimination of the CD4010A's. The waveforms for the R-2R network show a stepping input from zero to 12.8 volts divided into 100-millivolt steps. The CD4010A buffers may be used to permit lower R-2R values, if desired. Fig. 122 shows the logic diagram of the CD4020A 14-stage binary counter. Applications of the CD4020A are similar to those of the CD4024A.



*SYSTEM RESET ON COMPARISON TO PERMIT REPETITIVE OPERATOR FOR SCOPE DISPLAY.

**DIFFERENT ANALOG VOLTAGE RANGES CAN BE REALIZED BY DIFFERENT RESISTOR, COMPARATOR ARRANGEMENTS.

(a)



***1 VOLT/DIV VERTICAL SCALE.

(b)

Fig. 120 - (a) CD4024AE and weighted resistor network in an analog-to-digital conversion application; (b) waveforms at various circuit points.

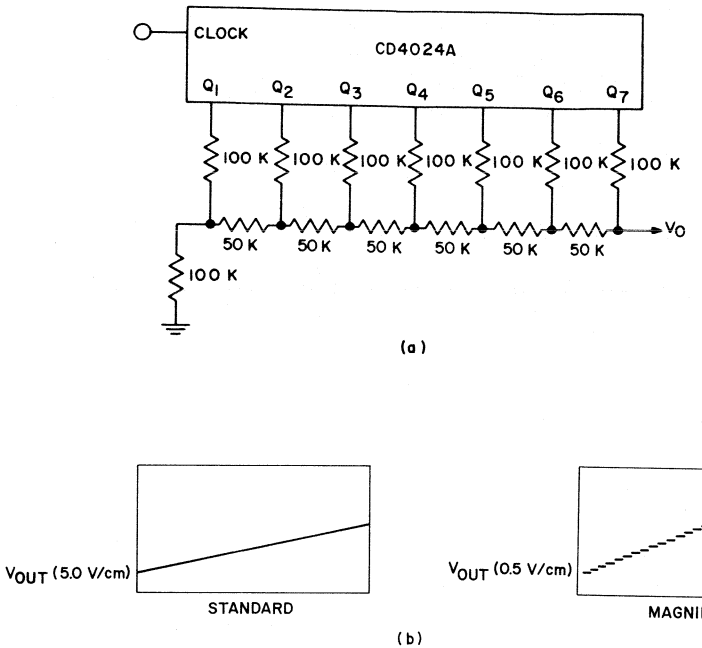


Fig.121 - (a) 4024A and R-2R ladder network in an analog-to-digital conversion application; (b) standard and magnified representations of the input waveform.

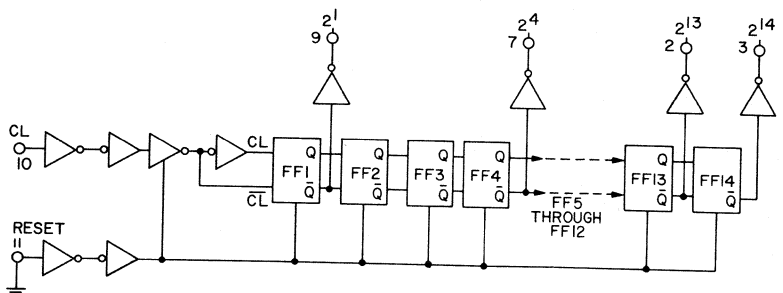


Fig.122 - CD4020A 14-stage binary counter.

DECADE COUNTER PLUS 10 DECODED DECIMAL OUTPUTS (CD4017A)

Fig. 123 shows the logic diagram of the CD4017A, a decade counter plus 10 decoded decimal outputs. A five-stage Johnson counter configuration is used to implement the decade counter. The basic flip-flop stages are similar to that described in Fig. 110. Clock, reset, inhibit, and carry out signals are provided. The decade counter advances one count at the positive clock-signal transition provided the inhibit signal is low. Counter advancement by way of the

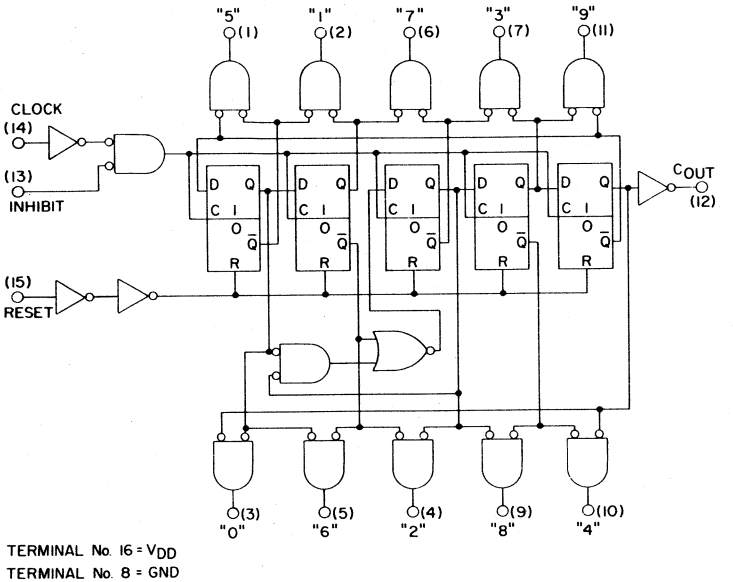


Fig.123 - CD4017A decade counter plus 10 decoded decimal outputs.

clock line is inhibited when the inhibit signal is high. A high reset signal clears the decade counter to its zero count. Use of the Johnson decade-counter configuration permits high-speed operation, two-input decimal-decode gating, and spike-free decoded outputs. Anti-lock gating is provided to permit only the proper counting sequence. The ten decimal outputs are normally low and go high only at their respective decoded-decimal time slot. Each decimal output remains high for one full clock cycle. The carry-out signal completes one cycle for every ten clock input cycles and is used to clock the following decade directly in any multi-decade application.

Fig. 124 shows the CD4017A in a multi-decade counter/decimal display application. Two typical lamp-driver interface circuits are shown. When one-sixth of a CD4009A is used as the lamp driver, current ranges up to 20 milliamperes and 7.5 milliamperes can be realized for COS/MOS supply voltages of 10 volts and 5 volts, respectively. Fig. 125 illustrates the use of the CD4017A in a multi-decade frequency-division application; decimal display is optional. Figs. 126, 127, and 128 show the use of the CD4017A to obtain various divide-by-N counter configurations. Figs. 126 and 127 illustrate two reset methods used in counting to the number 60; Fig. 128 shows an example of the divide-by-60, divide-by-60, and divide-by-24 configuration, and Fig. 129 shows the waveforms for this configuration. The CD4017A permits easy decimal display of each divide-by-N section. The CD4017A can also be used in applications requiring multiplexing, demultiplexing, and commutation of signals.

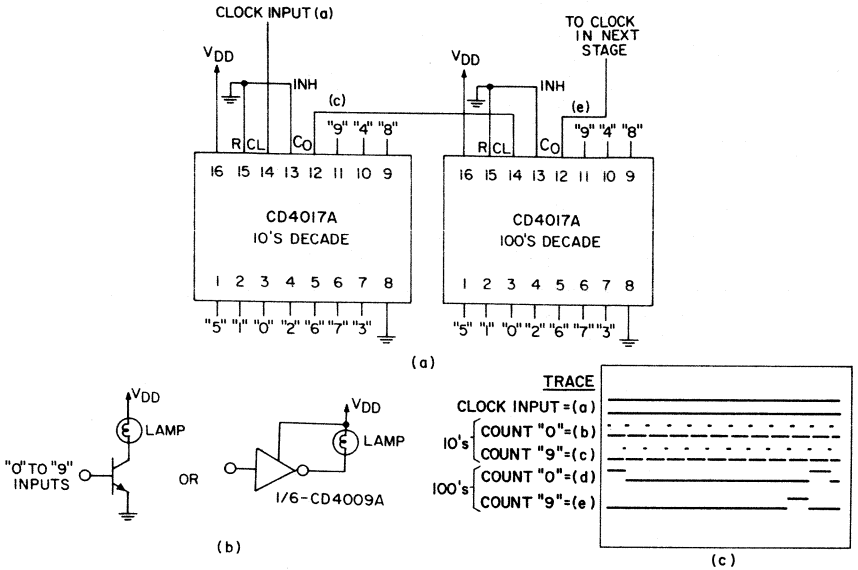


Fig.124 - (a) CD4017A multi-decade-counter/decimal display; (b) typical lamp-driver interface circuits; (c) circuit waveforms.

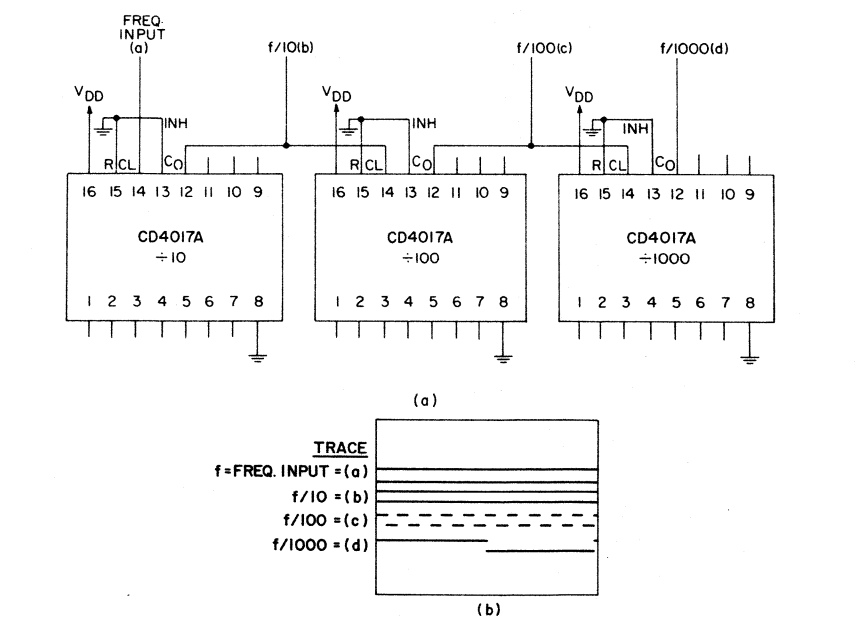


Fig.125 - (a) CD4017A multi-decade frequency-division application; (b) circuit waveforms.

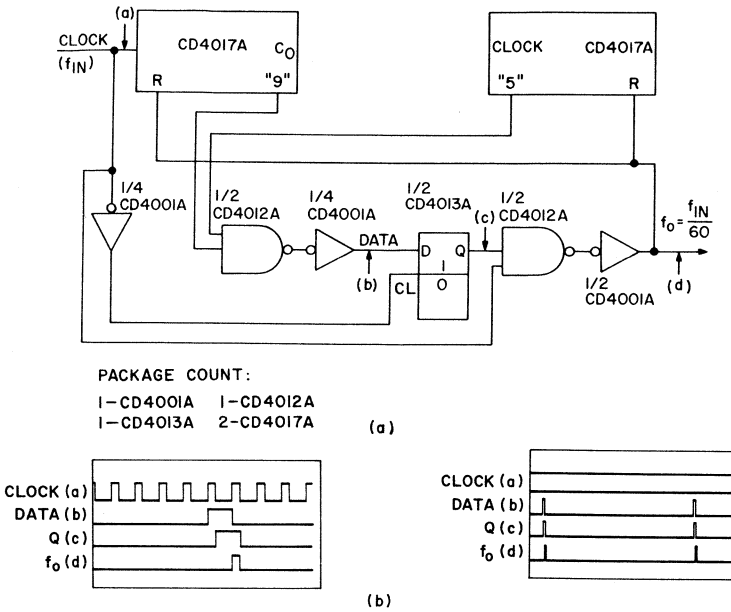


Fig.126 - (a) Divide-by-60 circuit using the CD4017A and reset mode 1; (b) circuit waveforms.

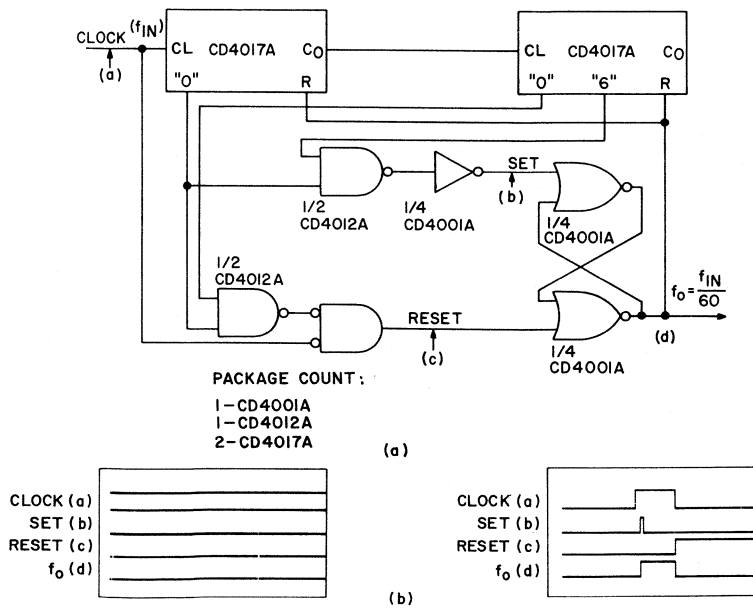


Fig.127 - (a) Divide-by-60 circuit using the CD4017A and reset mode 2; (b) circuit waveforms.

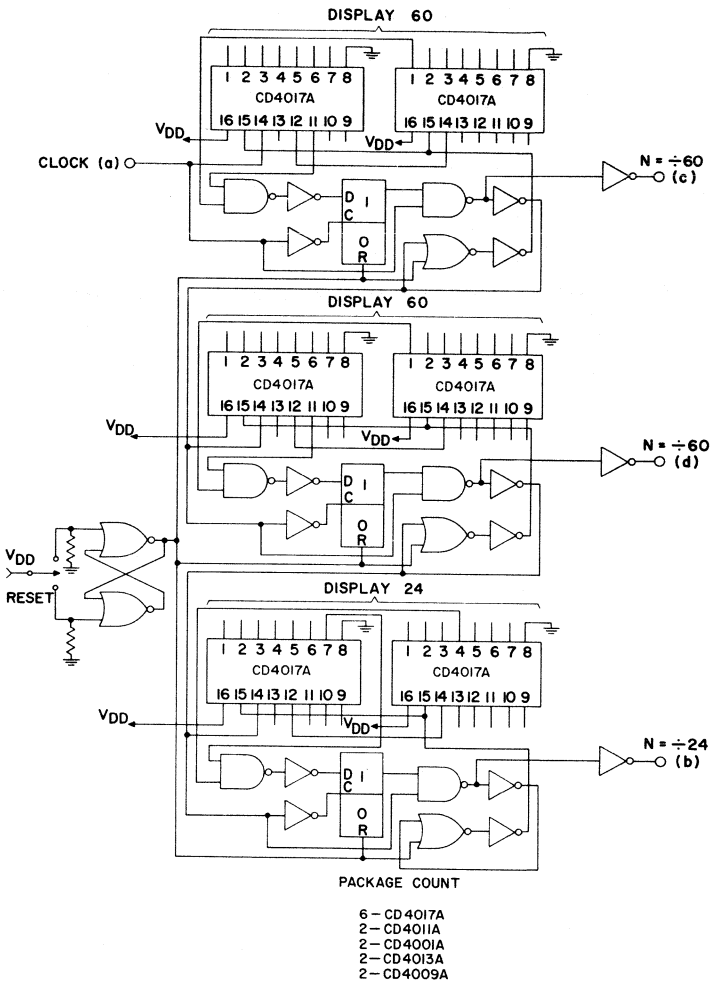


Fig.128 - Divide-by-60, divide-by-60, and divide-by-24 sections of a CD4017A divide-by-N counter.

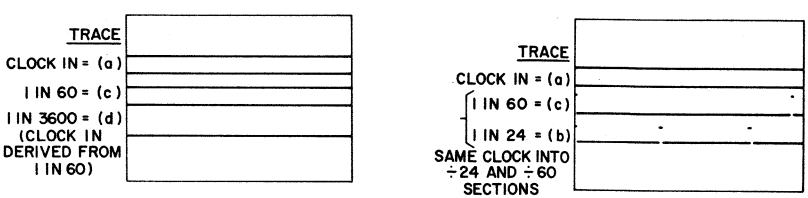


Fig.129 - Circuit waveforms for counter circuit shown in Fig. 128.

DIVIDE-BY-8 COUNTER AND 8 DECODED OUTPUTS (CD4022A)

Fig. 130 shows the logic diagram of the CD4022A, a divide-by-8 counter and 8 decoded outputs. A four-stage Johnson counter is used to implement the divide-by-8 counter. The basic flip-flop stages are similar to that described in Fig. 110. Clock, clock-enable, reset and carry-out signals are provided on the divide-by-8 counter. The divide-by-8 counter is advanced one count at the positive clock-signal transition. A high reset signal returns the divide-by-8 counter to its zero count. Use of the Johnson divide-by-8 counter configuration permits high-speed operation, two-input decode gating, and spike-free decoded outputs. Anti-lock gating is provided to permit only the proper counting sequence. The eight decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. The carry-out signal completes one cycle for every eight clock input cycles, and is used to clock the following counter stage directly in multi-stage applications.

Fig. 131 shows the CD4022A in a divide-by-8 counter/decoder application. One CD4022A unit provides the counting as well as the decoding function. Fig. 132 shows a divide-by-64 counter/decoder application. Fig. 133 shows the logic diagram and waveforms for the counter/decoder. Again, the partial decode function performed by the CD4022A significantly simplifies the external gating to complete the 1-in-64 decode function. Other binary counter/decoder applications can be realized similarly.

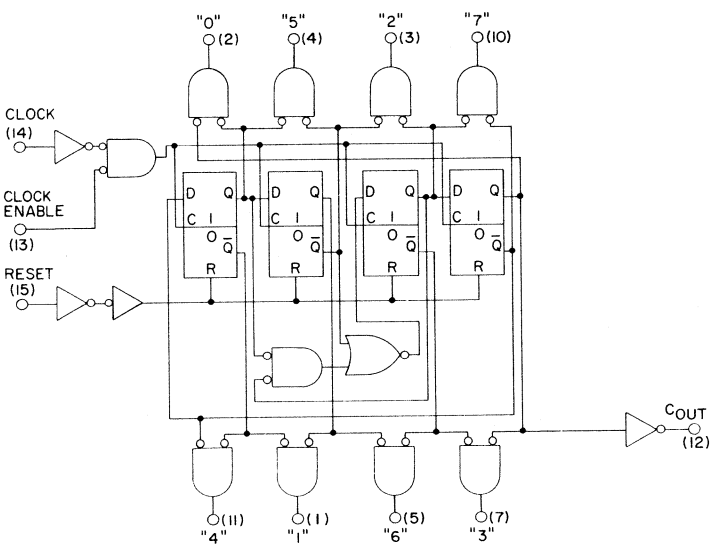


Fig. 130 - CD4022A divide-by-8 counter and 8 decoded outputs.

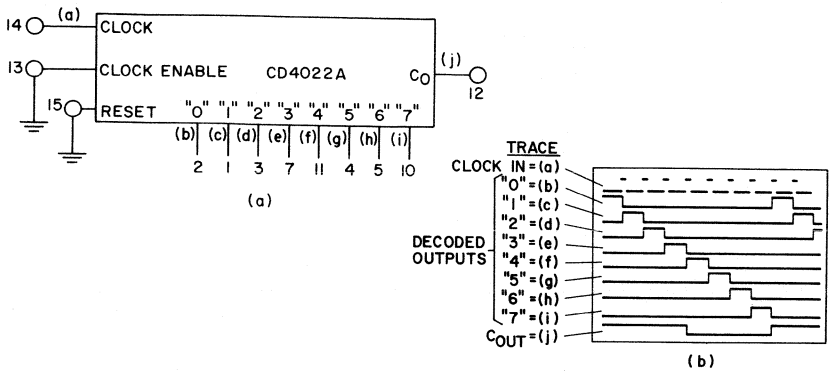


Fig.131 - (a) CD4022A divide-by-8 counter/decoder; (b) circuit waveforms.

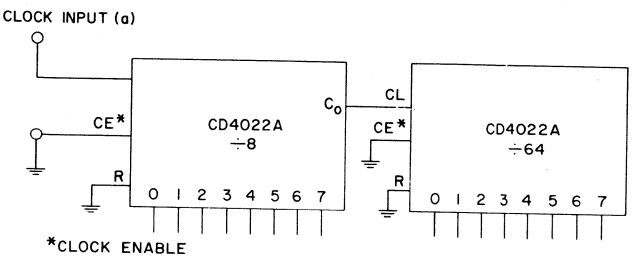


Fig.132 - CD4022A divide-by-64 counter/decoder.

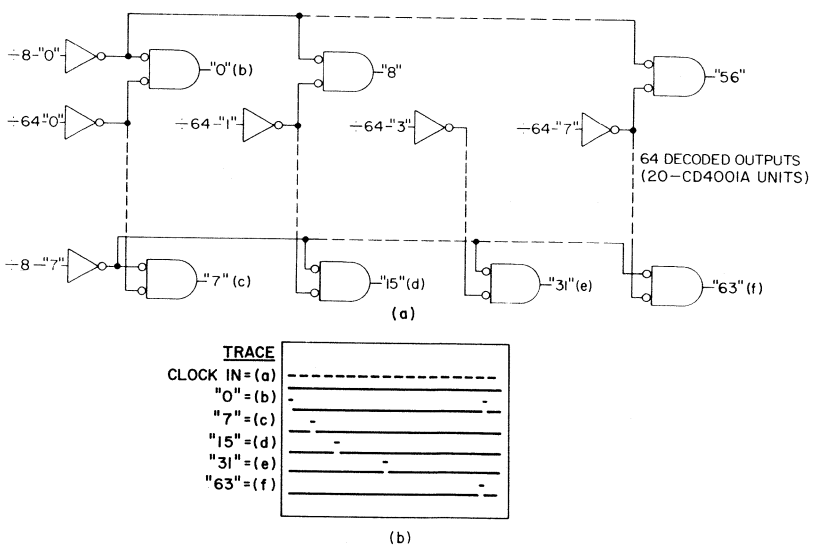


Fig.133 - (a) Logic diagram and (b) circuit waveforms for CD4022A divide-by-64 counter/decoder.

PRESETTABLE AND FIXED SINGLE-STAGE DIVIDE-BY-N COUNTERS (CD4018A)

Fig. 134 shows the logic diagram of the CD4018A, a presettable divide-by-N counter. The CD4018A consists of five flip-flops which can be configured as a 5-, 4-, 3-, or 2-stage Johnson counter with buffered $\overline{Q}$ outputs from each stage and counter preset control gating. Clock, reset, data, preset, and 5 jam inputs are provided. $\overline{Q}$ outputs are provided from each of the five counter stages. The basic flip-flop stages are similar to that shown in Fig. 110. Divide-by-10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$ or $\overline{Q}1$ signals, respectively, back to the data input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of NOR- or NAND-gate packages to gate the proper feedback connection to the data input line. Fig. 135 shows the feedback connections for divide-by-9, 7, 5, and 3 functions using the CD4011A NAND gate as the feedback circuit.

Fig. 136 shows the divide-by-seven configuration in detail. The pertinent waveforms for this circuit are shown in Fig. 137(a), and the counting sequences for a divide-by-eight and a divide-by-seven configuration are shown in Fig. 137(b). Division of the clock frequency by seven is accomplished by altering the counting sequence so as to skip the "all zeros" state of a divide-by-eight counter. The divide-by-seven counting sequence proceeds as in a normal 4-stage Johnson counter until count 3 (0001), at which point $\overline{Q}3$ = 0 and $\overline{Q}4$ = 1. At this point, the CD4011A gates $\overline{Q}3$ and $\overline{Q}4$ to put a 0 on the data input to the first stage. Thus, count 4 will be 1000 instead of

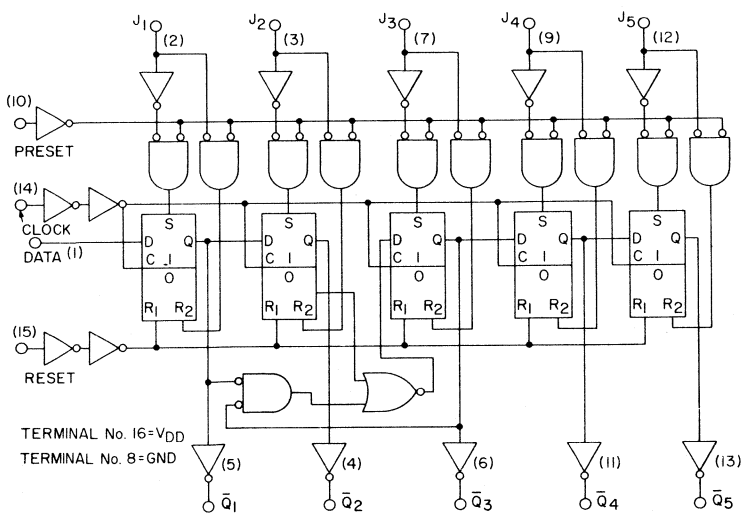


Fig. 134 - CD4018A presettable divide-by-N counter.

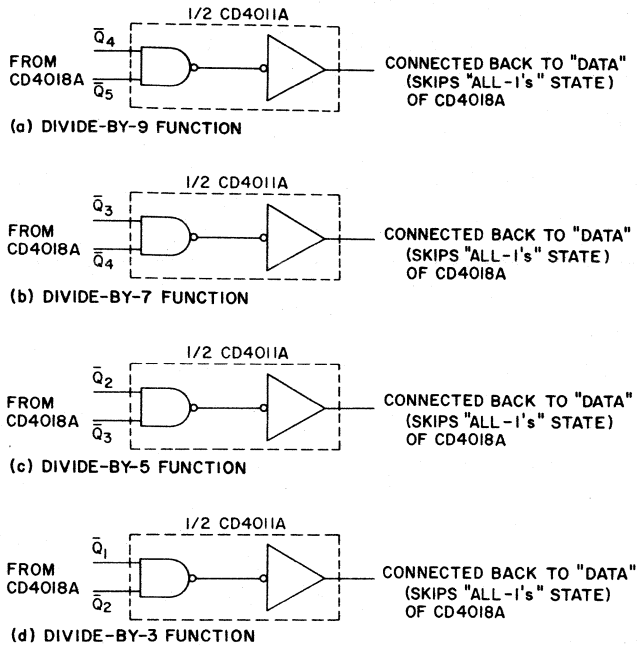


Fig.135 - External feedback connections for divide-by-9, 7, 5, and 3 functions using the CD4011A NAND gate.

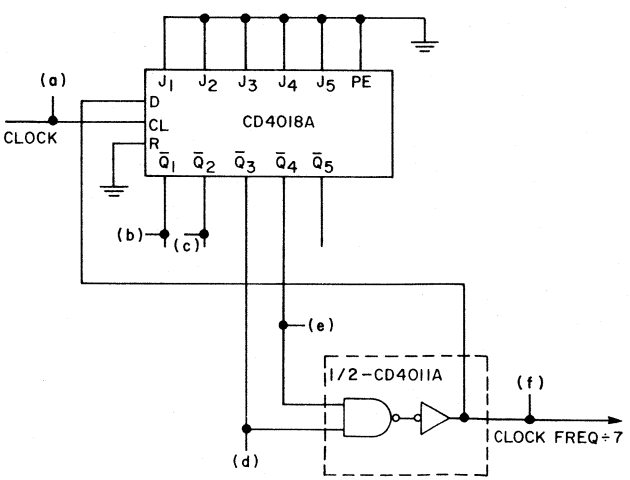
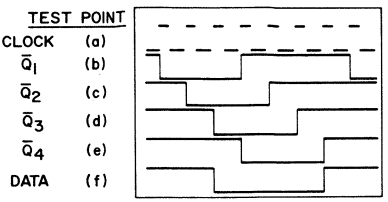


Fig.136 - CD4018A/CD4011A fixed divide-by-7 counter.



(a)

Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
0	1	1	1	1
1	0	1	1	1
2	0	0	1	1
3	0	0	0	1
4	0	0	0	0
5	1	0	0	0
6	1	1	0	0
7	1	1	1	0

Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
0	1	1	1	1
1	0	1	1	1
2	0	0	1	1
3	0	0	0	1
4	1	0	0	0
5	1	1	0	0
6	1	1	1	0

(b)

Fig. 137 - (a) Circuit waveforms; (b) counting sequences for a divide-by-8 and a divide-by-7 Johnson counter using the CD4018A.

0000 as in the unaltered divide-by-eight sequence. The remainder of the counting sequence proceeds in the normal 4-stage manner.

Divide-by functions greater than 10 can be achieved by use of multiple CD4018A packages. The counter configuration is advanced one count at the positive clock-signal transition. A high reset signal clears the counter to an all-zero condition. A high preset signal allows information on the jam inputs to preset the counter configuration. Anti-lock gating is provided to assure the proper counting sequence. The CD4018A can also be utilized as a five-stage parallel input/output holding register. Holding-register parallel entry can be controlled by means of the preset enable line, resulting in a five-stage latch operation.

PROGRAMMABLE MULTI-DECADE DIVIDE-BY-N COUNTERS

The CD4018A is especially useful in applications requiring low-power, programmable, divide-by-N counting. Two such applications are channel-preset counters in digital frequency synthesizers and program-counter control.

Fig. 138 illustrates the use of three CD4018A units in a programmable divide-by-N counter, where N may be any number from 2 to 999 (counter output is equal to clock frequency divided by N). Extension to higher N ranges is readily accomplished by the use of additional CD4018A units. The counter is preset to the value of N by use of the three selector switches. The switches are arranged so that switch position 9 is equivalent to a 0 count in the counter, position 8 is equivalent to a 1 count, position 7 to a 2 count, and so on. The counter counts up from the preset value (the N value) to its maximum count (999) and recycles, starting again from the preset value. Fig. 139(a) shows the counting sequence; oscillograph photographs of the waveform at various points in the circuit of Fig. 138 are shown in Fig. 139(b). Fig. 139(c) shows the N-counter output for various values of N.

The Johnson-counter configuration utilized in the CD4018A design permits significantly simpler program-switch (N-select) implementation than is required in systems

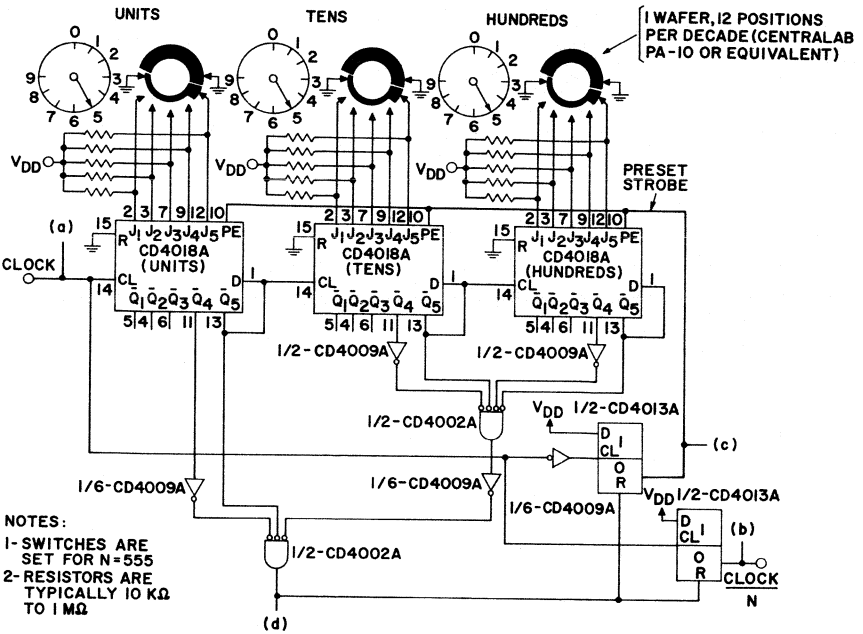


Fig.138 - CD4018A programmable divide-by-N counter application, N = 2 to 999.

FIRST DECADE (UNITS)							SECOND DECADE (TENS)							THIRD DECADE (HUNDREDS)						
SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$
9	0	1	1	1	1	1	9	0	1	1	1	1	1	9	0	1	1	1	1	1
8	1	0	1	1	1	1	8	1	0	1	1	1	1	8	1	0	1	1	1	1
7	2	0	0	1	1	1	7	2	0	0	1	1	1	7	2	0	0	1	1	1
6	3	0	0	0	1	1	6	3	0	0	0	1	1	6	3	0	0	0	1	1
5	4	0	0	0	0	1	5	4	0	0	0	0	1	5	4	0	0	0	0	1
4	5	0	0	0	0	0	4	5	0	0	0	0	0	4	5	0	0	0	0	0
3	6	1	0	0	0	0	3	6	1	0	0	0	0	3	6	1	0	0	0	0
2	7	1	1	0	0	0	2	7	1	1	0	0	0	2	7	1	1	0	0	0
1	8	1	1	1	0	0	1	8	1	1	1	0	0	1	8	1	1	1	0	0
0	9	1	1	1	1	0 *	0	9	1	1	1	1	0 *	0	9	1	1	1	1	0 *

* These digits, representative of count 9 in each decade, are decoded to give the preset strobe.

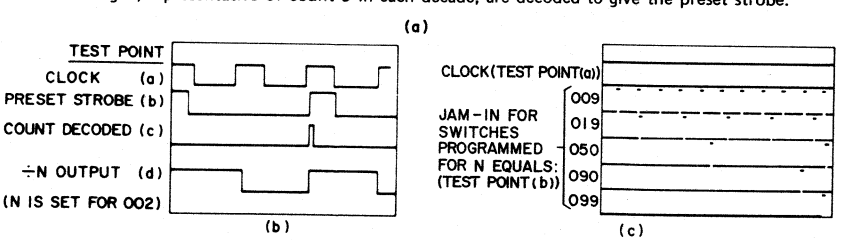


Fig.139 - (a) Counting sequence; (b) circuit waveforms; (c) circuit output for various values of N for circuit shown in Fig. 138.

that use a BCD decade-counter arrangement. The program switch is composed of three standard single-wafer switches, one for each CD4018A (one per decade), as compared with a four-wafer (4-pole) switch per decade for a BCD decade-counter arrangement. Also, the count decoding is much simpler in that only two outputs per CD4018A must be decoded as compared to four for a BCD arrangement. The Johnson-type counter can also operate at higher speeds and provide spike-free decoded outputs.

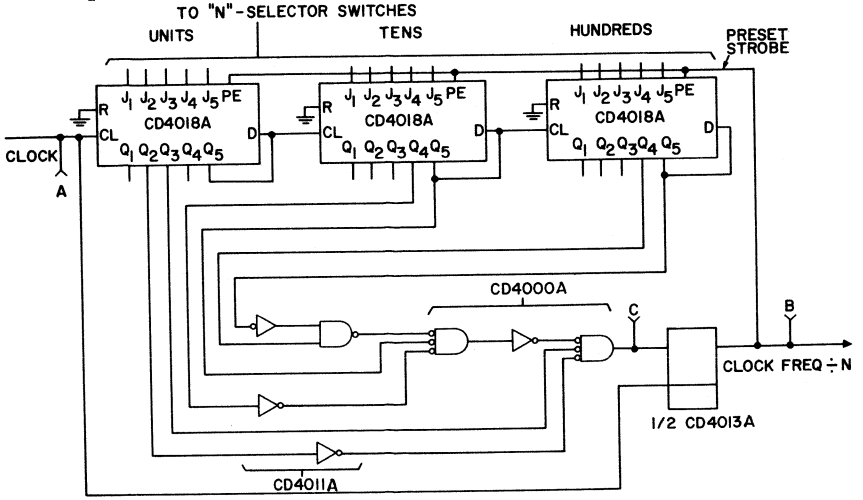


Fig. 140 - CD4018A programmable divide-by-N application (N = 3 to 999).

The configuration shown in Fig. 138 permits frequency division by 2 as a result of performing the preset function during half a clock cycle. In this mode, the maximum allowable frequency of operation is reduced, however. If this reduction in frequency is not acceptable, the logic diagram shown in Fig. 140 can be employed. In this circuit, the preset function is allowed a full clock cycle, but the range of frequency division is reduced to 3 to 999. The counting sequence and pertinent timing waveforms for this circuit are shown in Figs. 141(a), (b), and (c), respectively. Typical maximum operating frequency is 4 MHz for the counter in Fig. 138, and 6 MHz for the counter in Fig. 140.

PROGRAM-SWITCH (IN-SELECT) OPTIONS

Fig. 142 is a detailed drawing of a standard Centralab 12-position wafer switch and the associated resistor network as used in Fig. 138. The resistors connected to V_{DD} are required to prevent floating inputs on the jam lines. In applications that require lower power dissipation or where component count or space considerations become important, the resistor network can be eliminated by the redesign of the switch. Two such options are shown in Figs. 143 and 144, two-wafer-per-decade and single-wafer-per-decade switch configurations, respectively.

FIRST DECADE (UNITS)							SECOND DECADE (TENS)							THIRD DECADE (HUNDREDS)						
SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$
9	0	1	1	1	1	1	9	0	1	1	1	1	1	9	0	1	1	1	1	1
8	1	0	1	1	1	1	8	1	0	1	1	1	1	8	1	0	1	1	1	1
7	2	0	0	1	1	1	7	2	0	0	1	1	1	7	2	0	0	1	1	1
6	3	0	0	0	1	1	6	3	0	0	0	1	1	6	3	0	0	0	1	1
5	4	0	0	0	0	1	5	4	0	0	0	0	1	5	4	0	0	0	0	1
4	5	0	0	0	0	0	4	5	0	0	0	0	0	4	5	0	0	0	0	0
3	6	1	0	0	0	0	3	6	1	0	0	0	0	3	6	1	0	0	0	0
2	7	1	1	0	0	0	2	7	1	1	0	0	0	2	7	1	1	0	0	0
1	8	1	1	1	0	0	1	8	1	1	1	0	0	1	8	1	1	1	0	0
0	9	1	1	1	1	0	0	9	1	1	1	1	0	0	9	1	1	1	1	0

NOTE: "N" IS SELECTED BY DIALING IN THE DESIRED PRESET COUNT INDICATED BY THE SWITCH SETTINGS: THE "9" COUNTS FROM THE SECOND AND THIRD DECADE (SHOWN AS 1 0) ARE GATED WITH THE "7" COUNT (SHOWN AS 1 0) FROM THE FIRST DECADE TO ACTIVATE THE "PRESET ENABLE", ONCE PER COUNTER CYCLE.

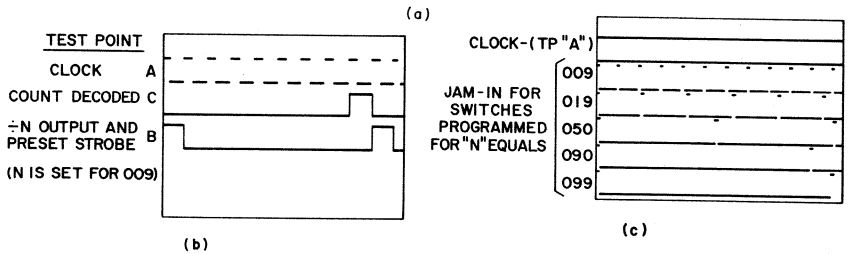


Fig.141 - (a) Counting sequence; (b) circuit waveforms; (c) circuit output (for various values of N) for programmable divide-by-N counter shown in Fig. 140.

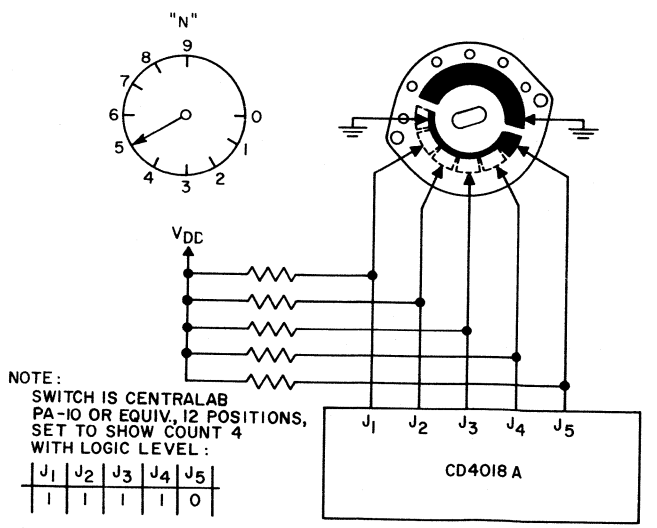


Fig.142 - Switch and resistor network used in circuit of Fig.138.

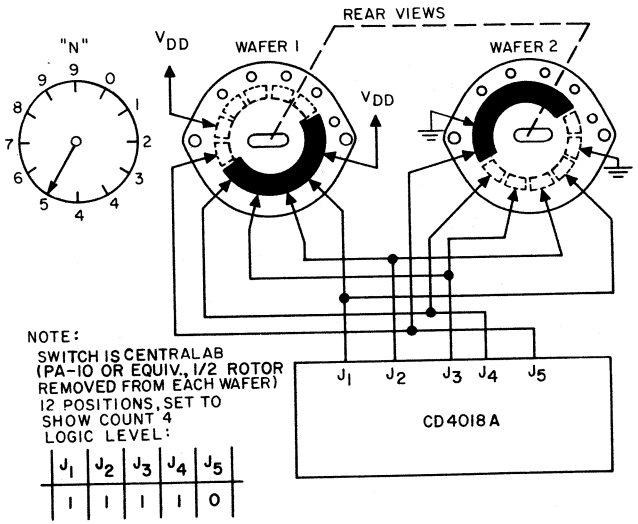


Fig.143 - Two-wafer-per-decade (modified standard) switch configuration.

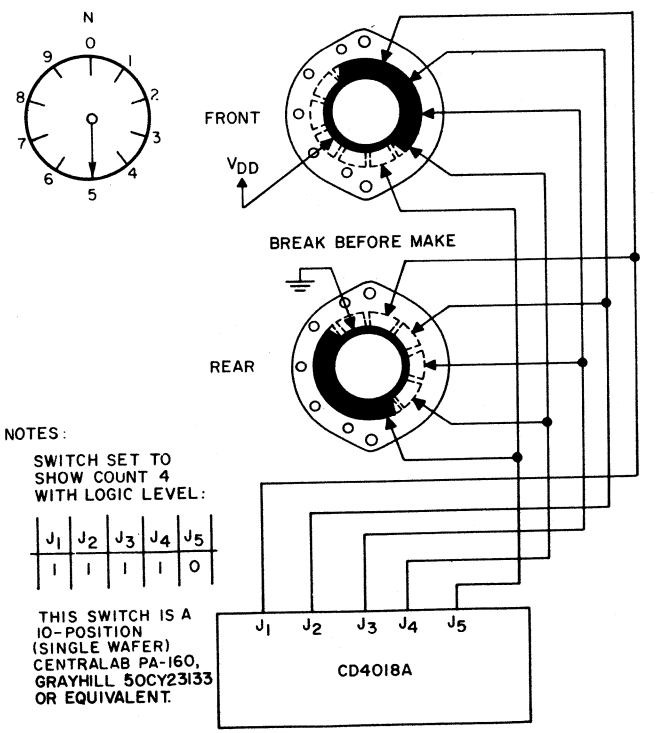


Fig.144 - Single-wafer-per-decade (nonstandard) switch configuration.

The range of N can be extended by adding more CD4018A units. In addition to this type of expansion, each stage in the programmable divide-by-N counter can be designed to count to any base or radix. For example, the single-stage divide-by-seven counter of Fig. 136 may be used as each stage in a multi-stage programmable counter.

18-STAGE STATIC SHIFT REGISTER (CD4006A)

Fig. 145 shows the logic diagram of the CD40006A, an 18-stage static shift register. The register stages are similar to those shown in Fig. 110. The CD4006A consists of four separate shift-register sections, two four-stage sections and two five-stage sections with output taps at the fourth stage. Each register section has independent data inputs to the first stage. The clock input is common to all 18 register stages. Through appropriate connection of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17, and 18 stages can be implemented using one CD4006A. Longer shift-register sections can be assembled by use of more than one CD4006A. Figs. 146 and 147 show the schematic and logic diagrams for one of the 18 register stages. Register shifting occurs on the negative clock-pulse transition.

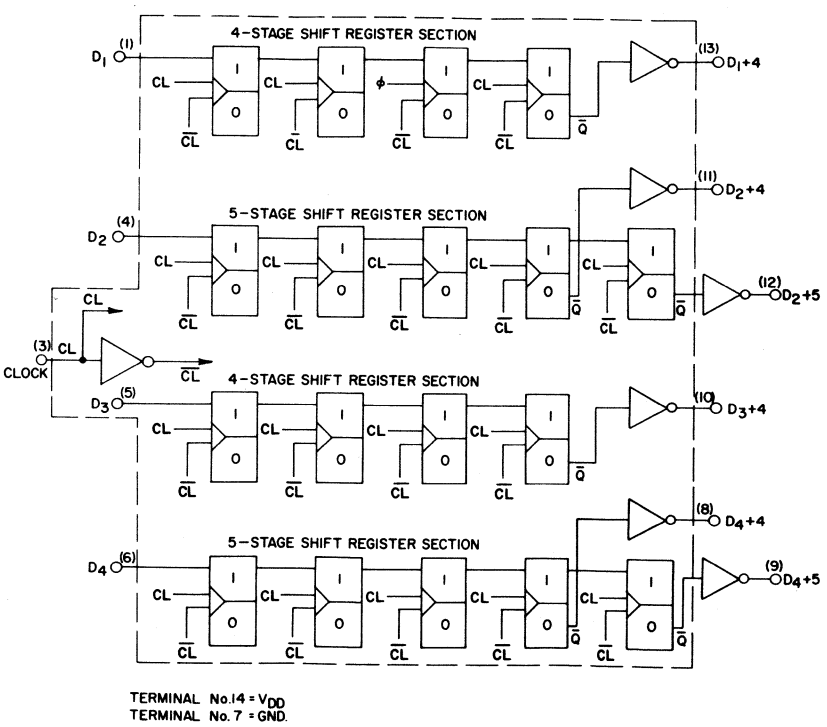


Fig. 145 - CD4006A 18-stage static shift register.

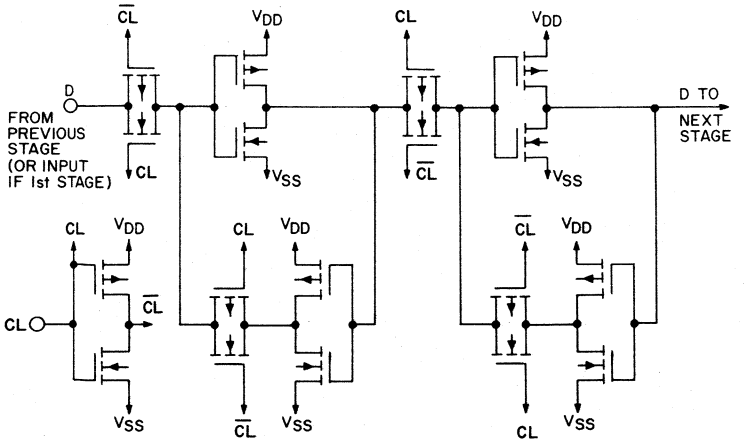


Fig. 146 - Schematic diagram for one of the 18 register sections of the CD4006A.

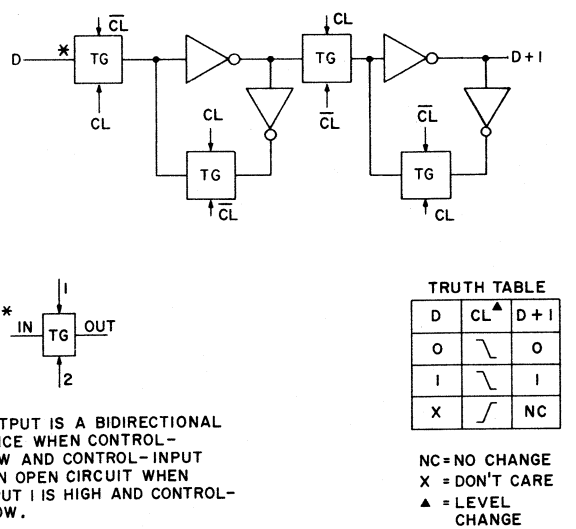


Fig. 147 - Logic diagram and truth table for one of the 18 register sections of the CD4006A.

DUAL 4-STAGE SERIAL-INPUT/PARALLEL-OUTPUT REGISTER (CD4015A)

Fig. 148 shows the logic diagram of the CD4015A, which consists of two identical, independent, four-stage serial-input/parallel-output registers. Each register has independent clock and reset inputs, as well as a serial data input. Q outputs are available from each of the four stages on both registers. All register stages are similar to that shown in Fig. 110. The logic level present at the data input is transferred into the first register stage and shifted over one stage at each positive clock transition. Reset of a four-stage section is accomplished by a high level on the reset line. Register expansion to 8 stages with one CD4015A or to more than 8 stages with multiple CD4015A packages is permitted.

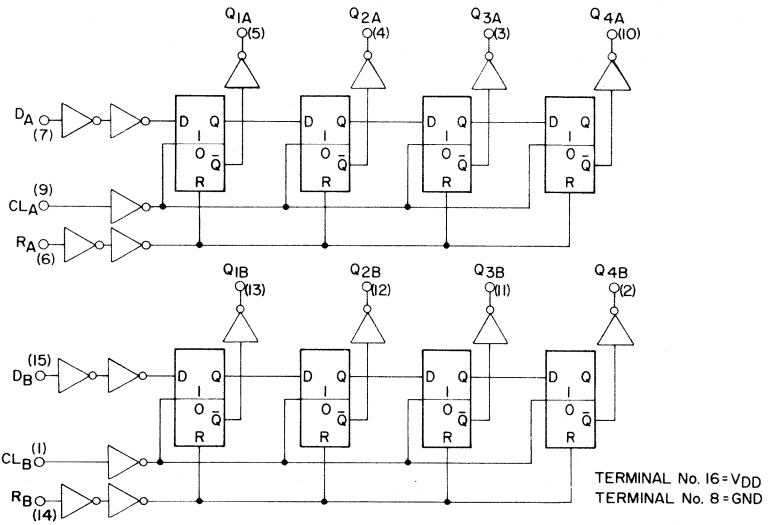


Fig. 148 - CD4015A dual 4-stage serial-input/parallel-output register.

Fig. 149 shows the use of the CD4015A in an 8-stage serial-input/parallel-output register application. This circuit operates as follows: The CD4015A connected as an 8-stage register is reset and 1's are shifted through the register. The scope trace in Fig. 150 shows the 1 pattern loading into the register until 1 reaches the eighth stage and initiates reset. After two clock pulses, the reset is removed and 1's again shift into the register. Low-speed-to-high-speed data queueing and serial/parallel data conversion are typical applications.

8-STAGE SYNCHRONOUS PARALLEL-INPUT/SERIAL-OUTPUT REGISTER (CD4014A)

Fig. 151 shows the logic diagram of the CD4014A, an 8-stage synchro-

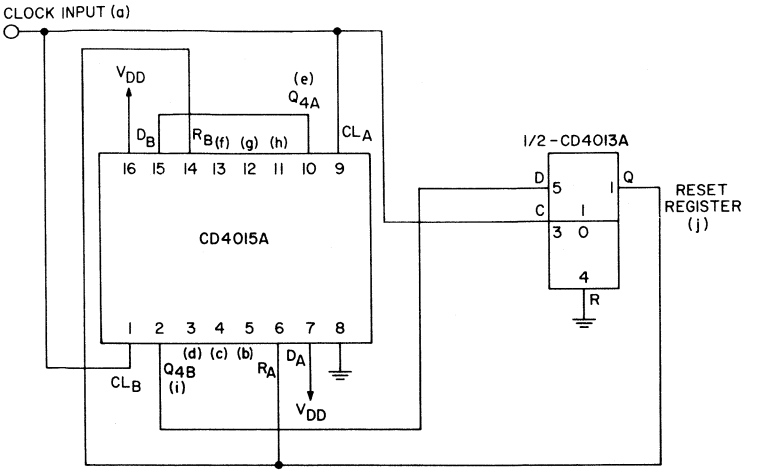


Fig. 149 - CD4015A 8-stage serial-input/parallel-output register application.

nous parallel-input/serial-output register. A clock input and a single serial data input together with individual parallel jam inputs to each register stage and a common parallel/serial control signal are provided. Q outputs from the 6th, 7th, and 8th stages are available. All register stages are similar to that shown in Fig. 110 except that extra transmission gates permit parallel or serial entry. Parallel or serial entry is made into the register synchronously with the positive clock transition and under control of the parallel/serial input.

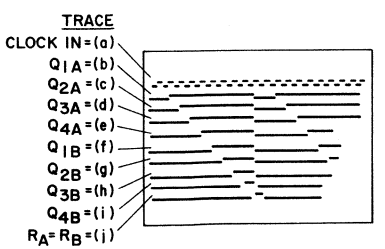


Fig. 150 - Waveforms for circuit shown in Fig. 149.

When the parallel/serial input is low, data is serially shifted into the 8-stage register synchronously with the clock positive transition. When the parallel/serial input is high, data is jammed into the 8-stage register by way of the parallel input lines and synchronously with the positive clock transition. Register expansion with multiple CD4014A packages is permitted. Fig. 152 shows the photomicrograph of the 82-mil by 84-mil CD4014A pellet.

Fig. 153 shows the CD4014A in an 8-stage synchronous parallel-input/serial-output register application. In this configuration, the CD4013A allows a parallel transfer to be made into the CD4014A register once every 8 clock pulses. Use of the divide-by-2 outputs of the CD4013A as parallel inputs to alternate CD4014A stages permits changeover from a 10101010 to a 01010101 parallel input pattern every 8 pulses. A scope trace of the changeover would show the parallel

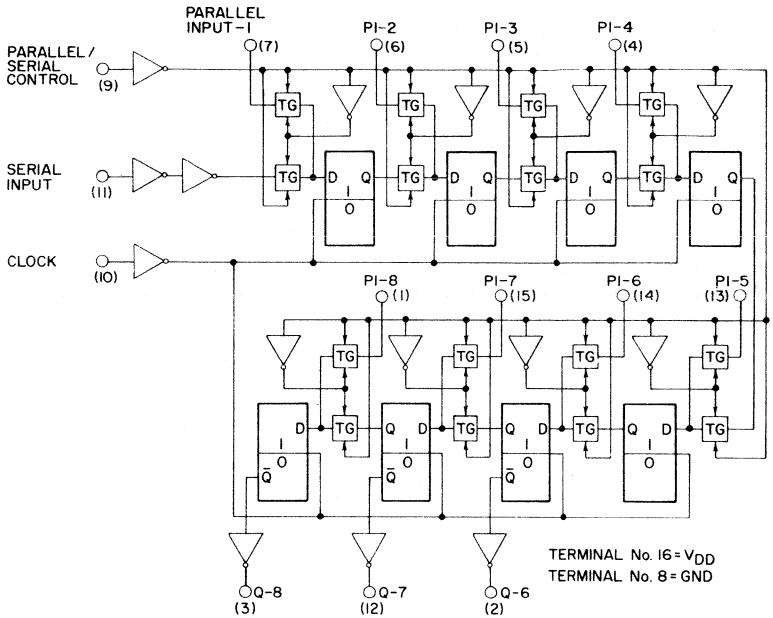


Fig.151 - CD4014A 8-stage synchronous parallel-input/serial-output register.

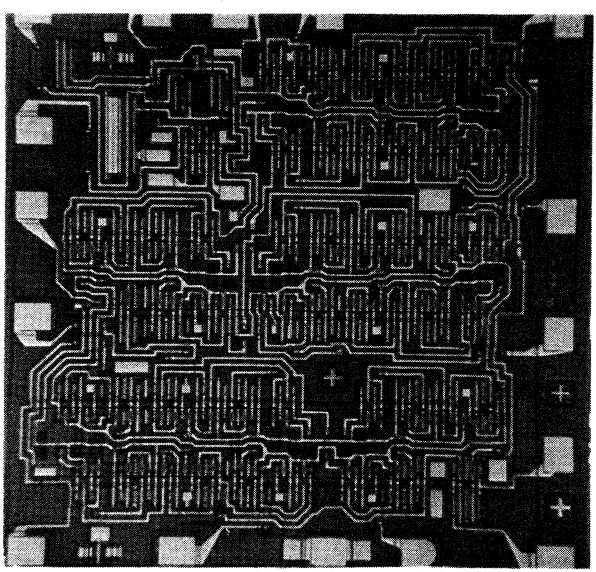


Fig.152 - Photomicrograph of the CD4014A pellet.

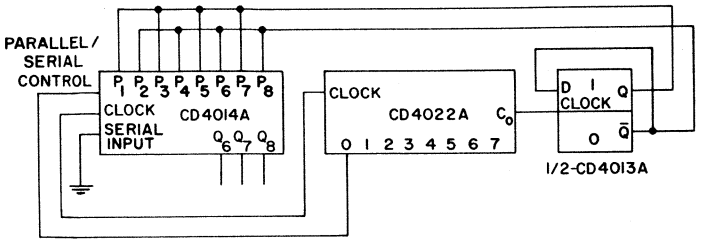


Fig. 153 - CD4014A 8-stage synchronous parallel-input/serial-output register application.

transfer of the 01010101 pattern into the register followed by eight shift pulses and subsequently another parallel transfer of 10101010 and eight shift pulses. High-speed-to-low-speed data queueing and parallel/serial data conversion are typical applications.

The CD4014A can be utilized in pseudo-random code-generation applications by means of combined control of the parallel input conditions and gating of the feedback of the 6th, 7th, and 8th stages to the serial input.

3-STAGE ASYNCHRONOUS PARALLEL-INPUT/SERIAL OUTPUT REGISTER (CD4021A)

Fig. 154 shows the logic diagram of the CD4021A 8-stage asynchronous parallel-input/serial-output reg-

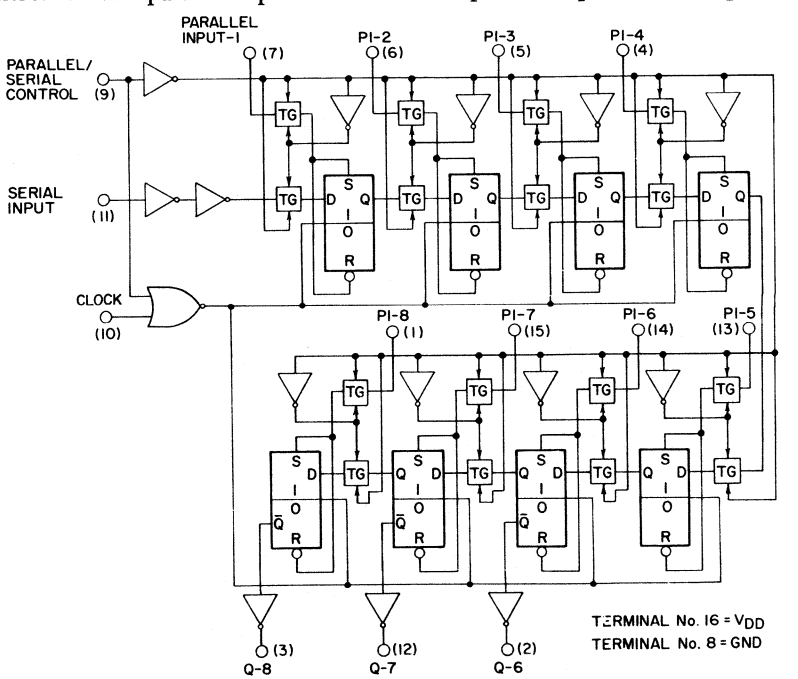


Fig. 154 - CD4021A 8-stage asynchronous parallel-input/serial-output register.

ister. Operation is basically the same as for the CD4014A except that parallel transfers are made as soon as the parallel/serial control input goes high. Parallel transfers are thus made asynchronously with the clock input. Serial shifting is still performed synchronously with the clock input. The CD4014A thus permits the parallel transfer to be synchronized with a different clocking signal than the serial transfer. In high-speed-to-low-speed data queueing, for example, an externally gated high-speed clock may control the parallel transfer while the low-speed clock controls the serial shifting.

Fig. 155 shows the CD4021A in an 8-stage asynchronous high-speed parallel-input/low-speed serial-output application, and Fig. 156 shows the logic diagram for this circuit. In the example shown, the high-speed portion of the system is simulated by simplified control logic. A 10-kHz low-speed clock and a 1-MHz high-speed clock are assumed. Signal lines a and b, as well as the eight data lines, are representative of the information transfer requirements between the high- and low-speed systems. Timing waveforms are shown in Fig. 157 for various points in the circuit of Fig. 156.

At the low-speed output section, the CD4021A shifts out stored information at a 10-kHz clock rate. The CD4022A counts to eight at the 10-kHz rate, and, at count zero, sends a high flag signal to the high-speed system over line (A). The flag signal indicates that the low-speed section is ready to accept eight bits on the data lines. In the simulated high-speed section, a high on line (A) allows flip-flop A to set on the positive transition of the 1-MHz clock. The Q output of flip-flop A is gated with the 1-MHz clock to form a gated 1-MHz clock signal on line (B). This clock signal, along with count zero at the low-speed section, puts a single 1-MHz gated clock pulse at the Parallel/Serial Control of the CD4021A to permit an eight-bit parallel transfer of data from the high-speed system to the low-speed system.

R-S flip-flops 1 and 2 remove the flag signal from line (A) after a 1-MHz gated clock pulse on line (B) has generated the parallel transfer signal. These flip-flops also prevent any further activation of line (A) and

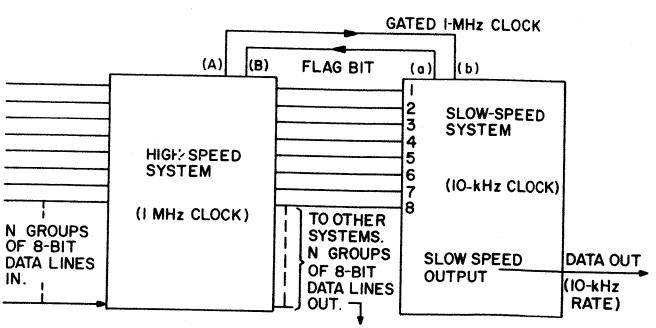


Fig. 155 - Block diagram of an 8-bit asynchronous high-speed-parallel-input/low-speed-serial-output application of the CD4021A.

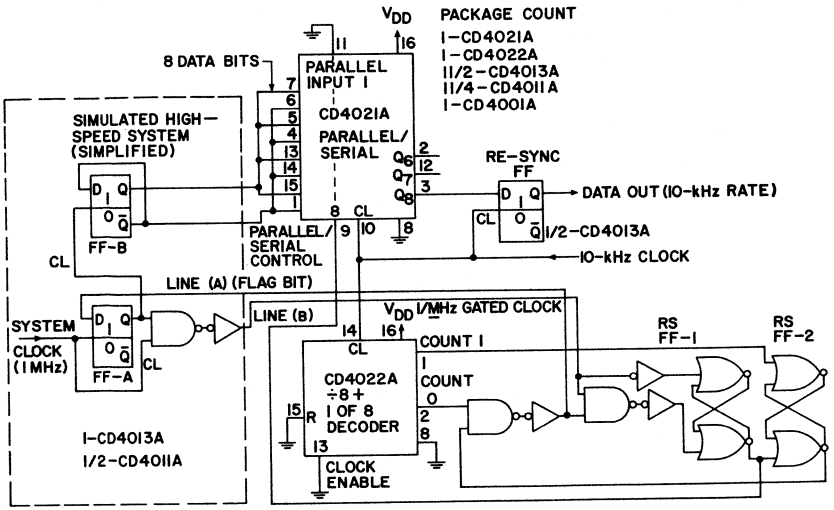


Fig.156 - Logic diagram of the 8-bit asynchronous high-speed-parallel-input/low-speed-serial-output application of the CD4021A shown in Fig. 155.

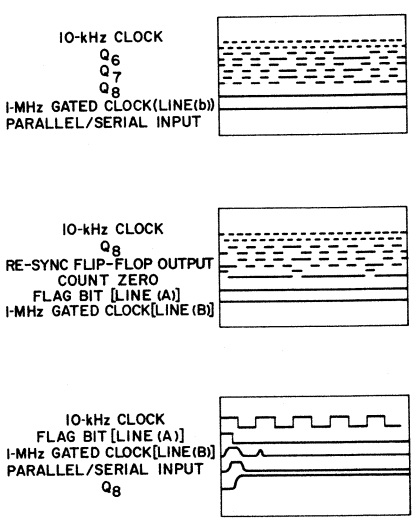


Fig.157 - Timing waveforms for the circuit of Fig. 156.

(B) and subsequent parallel transfers until the CD4022A counts back to zero. Thus, the eight bits transferred into the CD4021A are shifted out at the 10-kHz clock rate before a new set of data is transferred into the CD4021A. The extra pulse edge generated at line (B) (one clock pulse after the gated 1-MHz clock pulse) is ignored (see the logic of the low-speed section). For scope display purposes, flip-flop B in the high-speed system is used to change the pattern transferred every eight 10-kHz clock pulses from a 10101010 pattern to a 01010101 pattern.

In an actual system, the high signal at line (A) represents a flag bit that enables the high-speed system to transfer eight bits of new data at any time during the count zero (10-kHz clock-cycle duration). This feature allows the high-speed system time to service its many other input and output lines and to satisfy internal process requirements at the 1-MHz rate. At the same time, the high-speed system is still conditioning the eight transfer lines [just prior to activation of line (B)] with a pulse to enable the parallel transfer of data. The Re-Sync flip-flop in the low-speed section helps avoid any gap in the output data due to the variable delay possible in line servicing between the eighth bit shifted out of the CD4021A and the next parallel transfer of eight valid bits of information.

Digital Display Systems

The CD4026A and CD4033A COS/MOS decade counter/dividers are particularly suited for use in a variety of digital display systems, including battery-operated systems for digital clocks and watches, in which low power dissipation and low package count are important. Each circuit consists of a 5-stage Johnson decade counter and an output decoder that converts the Johnson code into a 7-segment decoded output to drive each stage of a numerical display. The CD4033A has ripple-blanking input and output (RBI and RBO) and lamp-test capability. The CD4026A has display-enable capability.

CIRCUIT OPERATION AND PERFORMANCE CHARACTERISTICS

The inputs to the CD4033A are clock, reset, clock enable, ripple-blanking input (RBI), and lamp test as shown in Fig. 158. The outputs are carry out, ripple-blanking output (RBO), and the seven decoded outputs (a,b,c,d,e,f,g). A high reset signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the clock-enable signal is low. Counter advancement by way of the clock line is inhibited when the clock-enable signal is high. A timing diagram for the CD4033A is shown in Fig. 159. Antilock gating is provided on the Johnson counter to assure proper counting sequence.

The carry-out (Cout) signal completes one cycle every ten clock input cycles and is used to clock the succeeding decade directly in a multi-decade counting chain. The seven decoded outputs (a,b,c,d,e,f,g) illuminate the proper segments in a 7-segment display device used to present the decimal number 0 to 9. The 7-segment outputs go "high" on selection.

The CD4033A has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number. This feature results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight-digit display would be displayed as 50.07. Zero suppression on

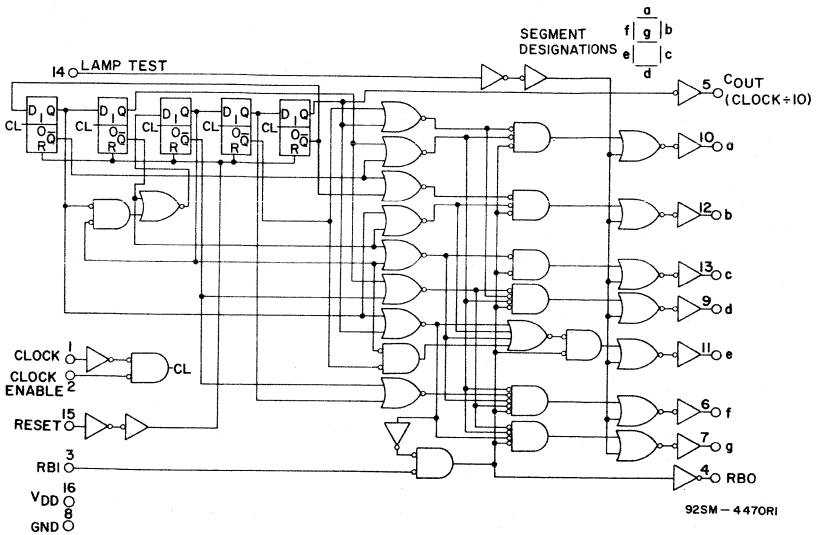


Fig. 158 - Logic diagram for CD4033A decade counter/divider with decoded 7-segment display outputs.

the integer side is obtained by the connection of the RBI terminal of the CD4033A associated with the most significant digit in the display to a low-level voltage and the connection of the RBO terminal of the same stage to the RBI terminal of the CD4033A in the next-lower-significant position in the display. This procedure is continued for each succeeding CD4033A on the integer side of the display.

On the fraction side of the display, the RBI of the CD4033A associated with the least significant bit is connected to a low-level voltage and the RBO of the same CD4033A is connected to the RBI terminal of the CD4033A in the next more significant-bit position. This procedure is continued for each CD4033A on the fraction side of the display.

In a purely fractional number (e.g. 0.7346), the zero immediately preceding the decimal point can be displayed by the connection of the RBI of that stage to a high-level voltage (instead of the RBO of the next more significant stage). Similarly, the zero in a number such as 763.0 can be displayed by the connection of the RBI of the CD4033A associated with it to a high-level voltage. Ripple blanking of non-significant zeros provides an appreciable savings of display power.

The CD4033A has a lamp-test input which, when connected to a high-level voltage, overrides normal decoder operation and enables a

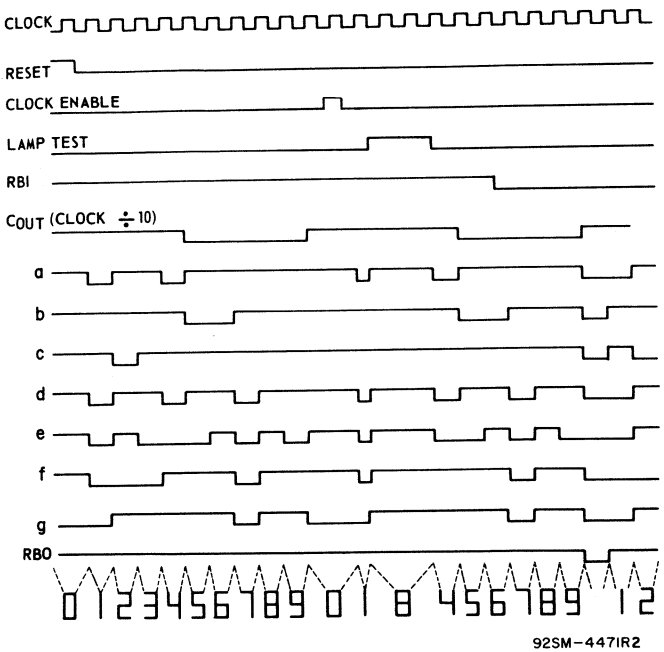


Fig.159 - CD4033A timing diagram.

check to be made of possible display malfunctions by putting the 7 outputs in the high state.

Fig. 160 shows the logic diagram of the RCA CD4026A. The CD4026A is identical to the CD4033A except that the ripple-blanking input (RBI) and the ripple-blanking output (RBO) and lamp-test capabilities are replaced by a "display enable" control. An extra c-segment output (not gated with the display enable) is available to retain the ability to implement the divide-by-12 function. The power dissipation and output characteristics of the CD4026A and CD4033A are identical.

DISPLAY DRIVERS

The decoded outputs of the CD4026A and CD4033A decade counter/dividers are applied to the segments of the digital display devices through display driving circuits. The following paragraphs briefly describe a pair of COS/MOS integrated circuits and a pair of bipolar integrated circuits suitable for use as display drivers.

COS/MOS IC Drivers (CD4009A and CD4010A)

Figs. 161 and 162 show the circuit diagrams for the CD4009A (Inverting Hex Buffer) and CD4010A (Non-Inverting Hex Buffer), respectively. Six buffers are provided per package. Figs. 163 and 164 show V_{OL} output characteristics (n-channel) and V_{OH} output characteristics (combined p-and-n-channel devices) for both types.

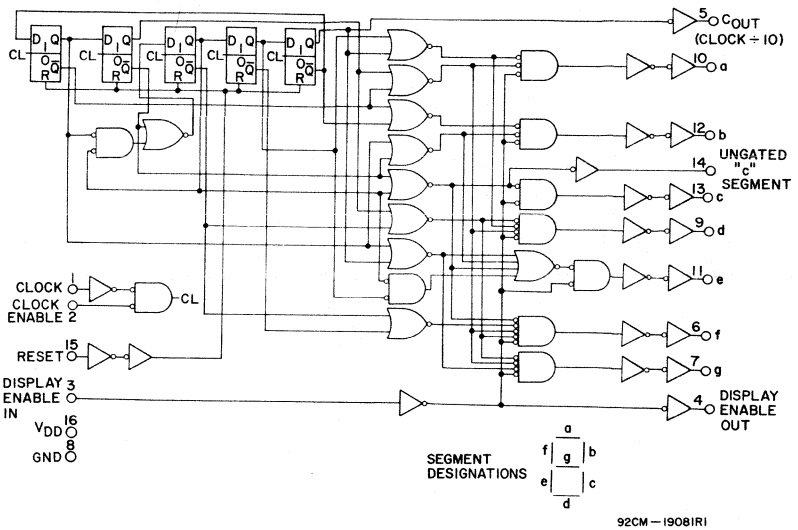


Fig. 160 - Logic diagram of CD4026A.

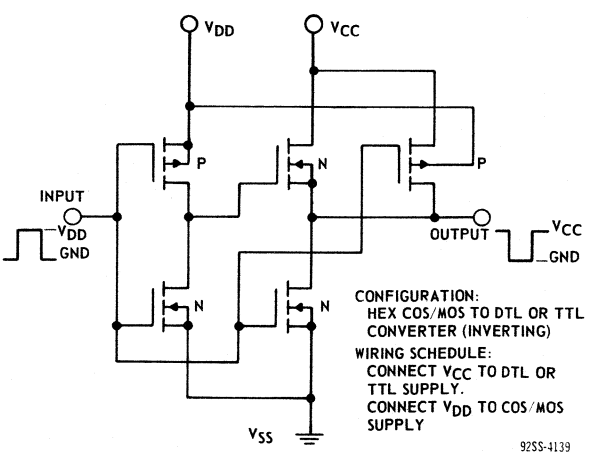


Fig. 161 - Schematic diagram (1 of 6 identical stages) of CD4009A.

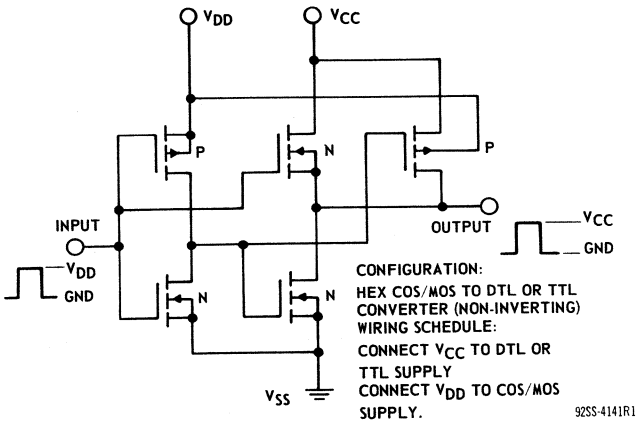
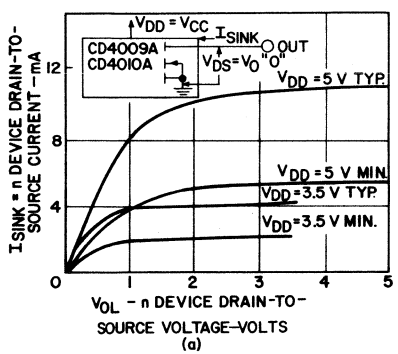
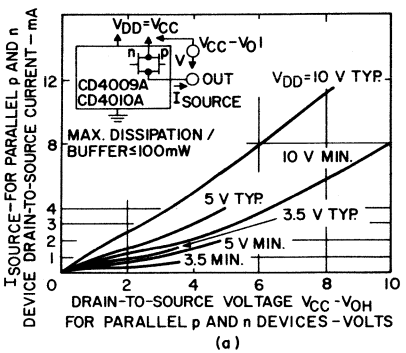
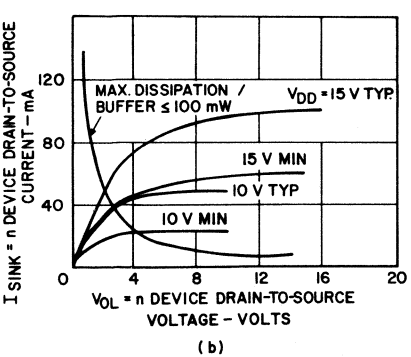


Fig.162 - Schematic diagram (1 of 6 identical stages) of CD4010A.







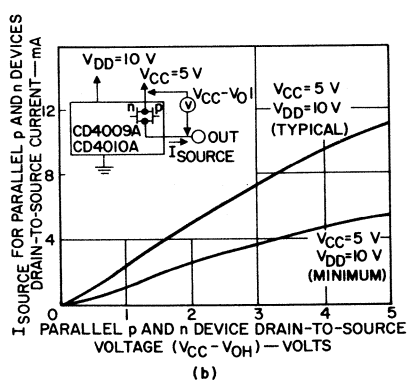
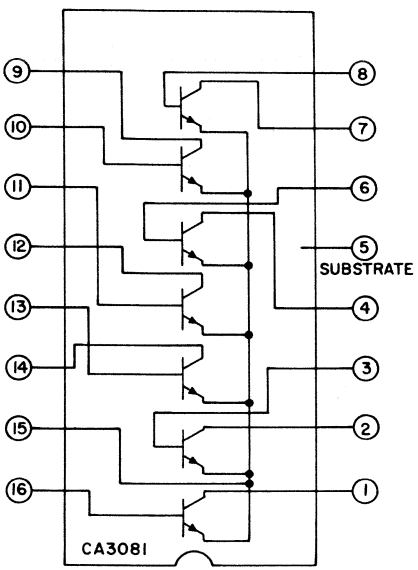


Fig. 163 - (a) CD4009A and CD4010A V_{OL} output drive capability, $V_{DD} = V_{CC}$ = 3.5, 5V; (b) CD4009A and CD4010A V_{OL} output drive capability, $V_{DD} = V_{CC}$ = 10, 15V.

Fig. 164 - (a) CD4009A and CD4010A $V_{CC}-V_{OL}$ output drive capability, $V_{DD} = V_{CC}$ = 10.5, and 3.5V; (b) CD4009A and CD4010A $V_{CC} - V_{OL}$ output drive capability, V_{DD} = 10V and V_{CC} = 5V.

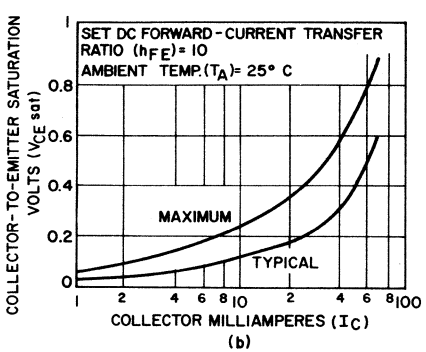
Bipolar IC Drivers (CA3081 and CA3082)

Fig. 165(a) shows the schematic diagram of the CA3081 (common-emitter array). Fig. 165(b) shows $V_{CE}(sat)$ as a function of collector current for one of 7 identical transistors.



COMMON-EMITTER CONFIGURATION

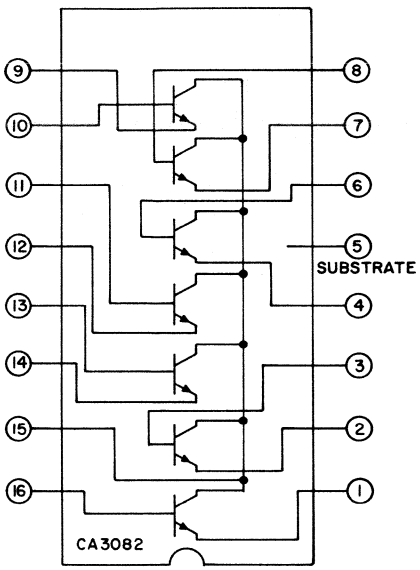
(a)



(b)

Fig. 165 - (a) Functional diagram CA3081; (b) $V_{CE}(sat)$ as a function of I_C at T_A = 25°C.

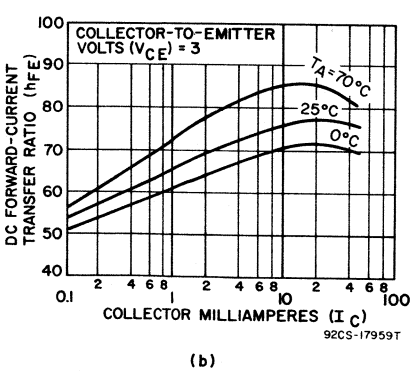
Fig. 166(a) shows the schematic diagram of CA3082 (common-collector array). Fig. 166(b) shows h_{FE} as a function of collector current at V_{CE} = 3V.



COMMON-COLLECTOR CONFIGURATION

(a)

92CS-17957



92CS-17959T

(b)

Fig. 166 - (a) Functional diagram of CA3082; (b) h_{FE} as a function of I_C.

INTERFACING DECADE COUNTER/DIVIDERS WITH DISPLAY DEVICES

The CD4016A and CD4033A decade counter/dividers can be used with most popular types of digital display devices. The following paragraphs describe the interfacing methods for various types of display devices.

Light-Emitting Diodes

The MAN 3 (Monsanto or equivalent) is a low-power monolithic, 7-segment diffused planar GaAsP light-emitting-diode display. Figs. 167(a) and 167(b) show the equivalent schematic and physical dimensions of the MAN 3. Fig. 168 shows brightness as a function of forward current. A fairly bright display (200 foot-lamberts) is achieved at a typical power dissipation of 8.5 milliwatts (1.7 volts x 5 milliamperes) per segment for a 100-per-cent duty-cycle drive mode. Greater display intensities can be realized by the use of higher-forward-current drives for a duty cycle of less than 100 per cent (i.e., light-enhancement factor equals direct current divided by pulsed

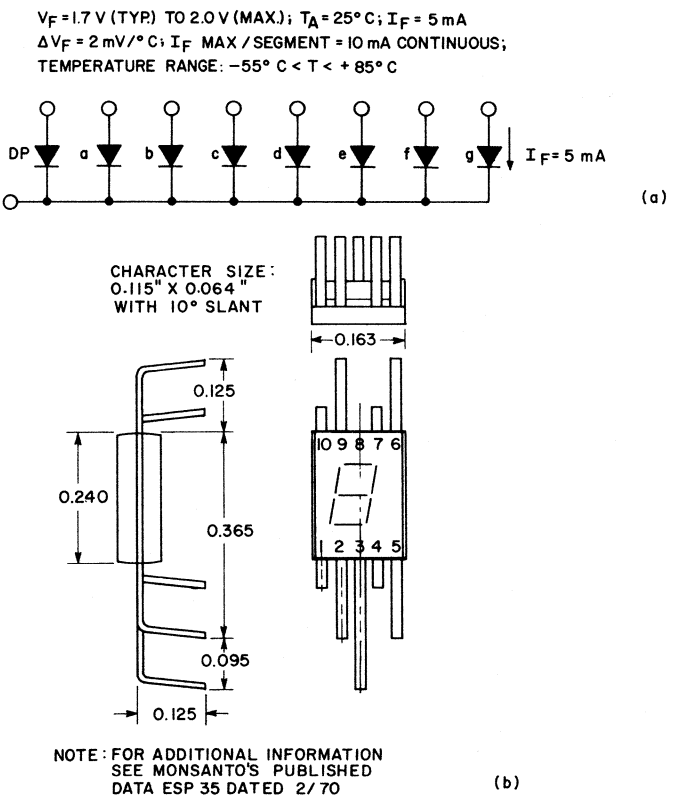


Fig. 167 - (a) Schematic diagram and (b) physical dimensions of the MAN-3 display device.

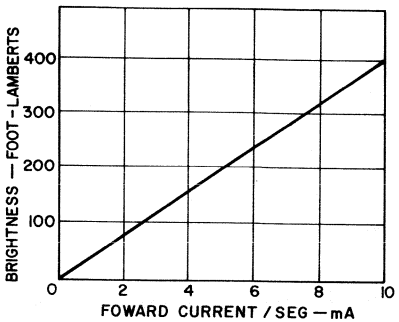


Fig. 168 - Brightness as a function of forward current for the MAN-3 display device.

current $I_{F(AV)}$ and is greater than unity, where both direct and pulsed current result in similar light intensity as seen by the human eye).

The requirement of lowest power at greatest light intensity makes it desirable to multiplex the display current between characters of a display, as well as between segments of a character. Display wiring may also be simplified by such multiplexing methods. Displays similar to MAN 3 characteristics, but containing multiple 7-segment display elements are available from Hewlett Packard and others. For example, Fig. 169 shows the approximate physical dimensions for the HP 5082 Series of LED's. The characteristics are similar to those of the MAN 3.

Fig. 170 shows techniques for

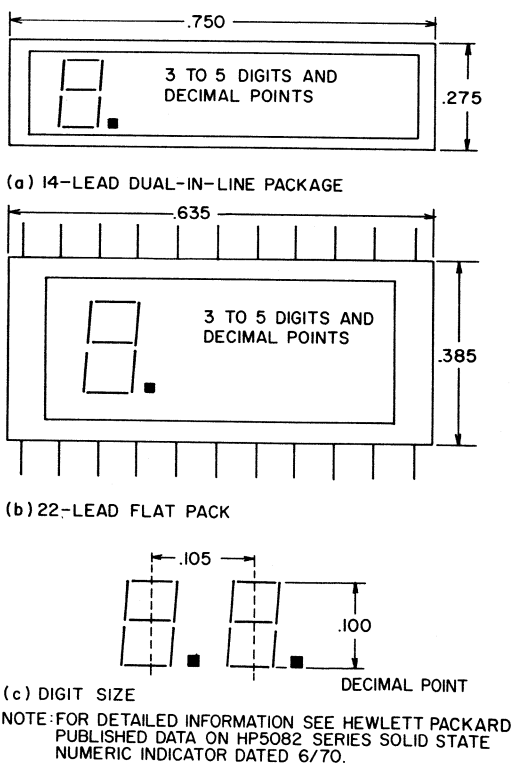


Fig. 169 - Package physical dimensions for HP5082.

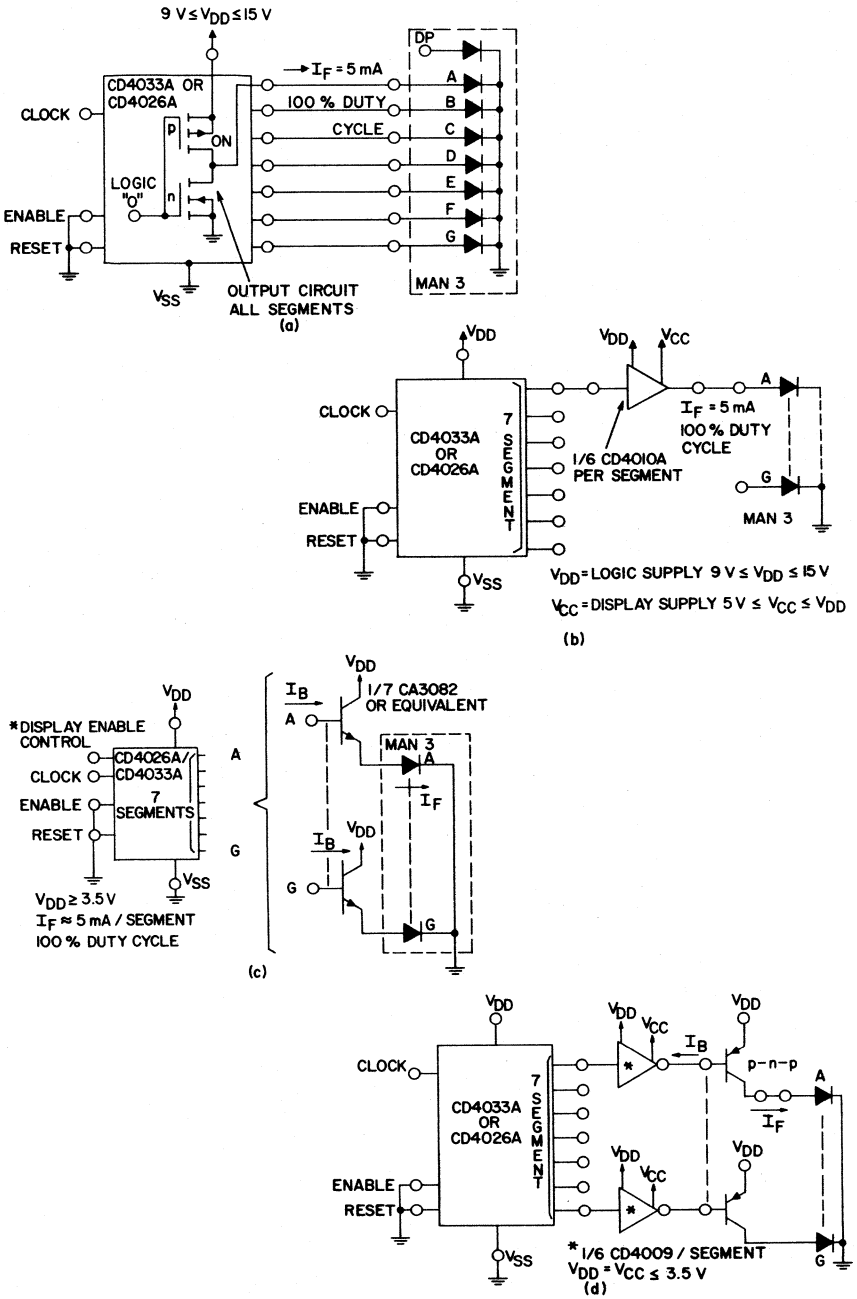


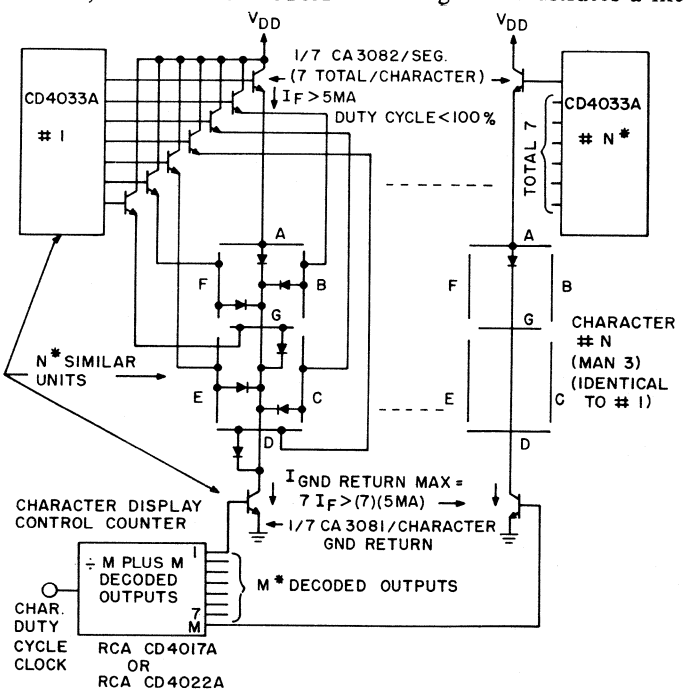
Fig.170 - CD4033A or CD4026A being interfaced with MAN-3 at various supply voltages.

the interface of the CD4033A or CD4026A to the MAN 3 display at various supply-voltage conditions. Fig. 170(a) shows a direct-drive condition at a duty cycle of 100 per cent for V_{DD} between 9 and 15 volts. A typical CD4033A can supply a forward current of 5 milliamperes per segment with a supply voltage as low as 9 volts and yields a fairly bright display. The power supply dissipation is approximately 45 milliwatts per segment (9 volts x 5 milliamperes).

For lower system power dissipation and separate logic and display supply sources, the RCA-CD4010A COS/MOS hex buffer package can be used, as shown in Fig. 170(b). In this case, the power supply dissipation per segment is less than 25 milliwatts (5 volts x 5 milliamperes).

For supply voltages as low as 3.5 volts, an n-p-n transistor array interface circuit is required as shown in Fig. 170(c). External base or emitter resistors may be used to obtain finer control of forward current, depending on the n-p-n array selected. For supply voltages less than 3.5 bolts, both the CD4009A and a p-n-p transistor array interface-circuit are required as shown in Fig. 170(d).

Fig. 171 illustrates a method for

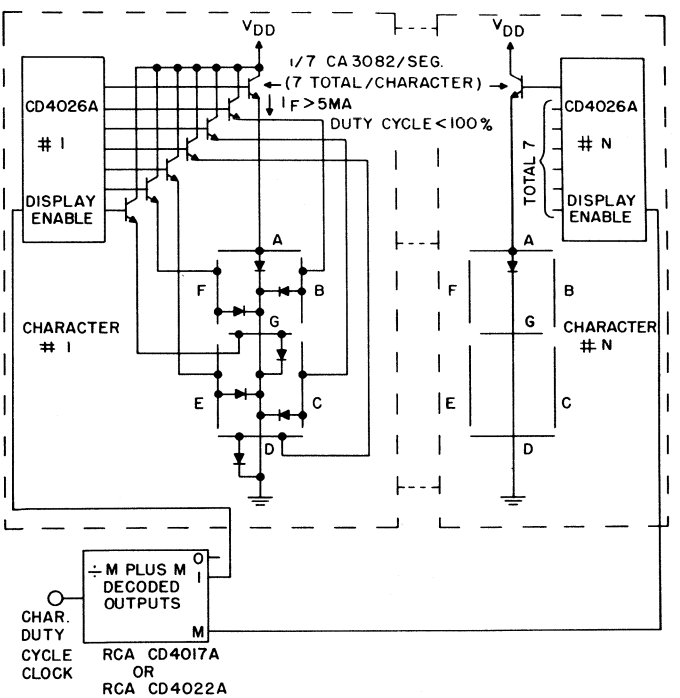


* N IS THE NUMBER OF CHARACTERS IN THE DISPLAY.

M IS THE NUMBER OF CHARACTER DISPLAY CONTROL COUNTER DECODED OUTPUTS. THE DISPLAY CONTROL COUNTER CLOCK AND THE VALUE OF M DETERMINES THE DISPLAY DUTY CYCLE OF THE CHARACTERS.

Fig. 171 - Character-display drive-multiplexing using the CD4033A and the MAN-3.

character-drive-multiplexing using the CD4033A. Character multiplexing and the use of higher forward-segment currents at less than 100-per-cent duty cycle permit light enhancement factors greater than 1 to be realized. This mode of operation (compared with the 100-per-cent duty-cycle mode, for the same display brightness) permits savings in display power dissipation. Fig. 172 shows a similar character multiplexing arrangement using the CD4026A. The multiplexing is accomplished at the logic level, as opposed to switching the display-character ground currents. A character display driver multiplexing circuit to interface the CD4026A with the HP5082 series multiple character display is shown in Fig. 173. A remetallization (not shown) of the CD4033A could be used to eliminate the n-channel device of all segment outputs. Elimination of the "N" channel device would permit direct connection of respective segments of all characters to the base of one



* N IS THE NUMBER OF CHARACTERS IN THE DISPLAY.

M IS THE NUMBER OF CHARACTER DISPLAY CONTROL COUNTER DECODED OUTPUTS. THE DISPLAY CONTROL COUNTER CLOCK AND THE VALUE OF M DETERMINES THE DISPLAY DUTY CYCLE OF THE CHARACTERS.

Fig. 172 - Character-display drive-multiplexing using the CD4026A and the MAN-3.

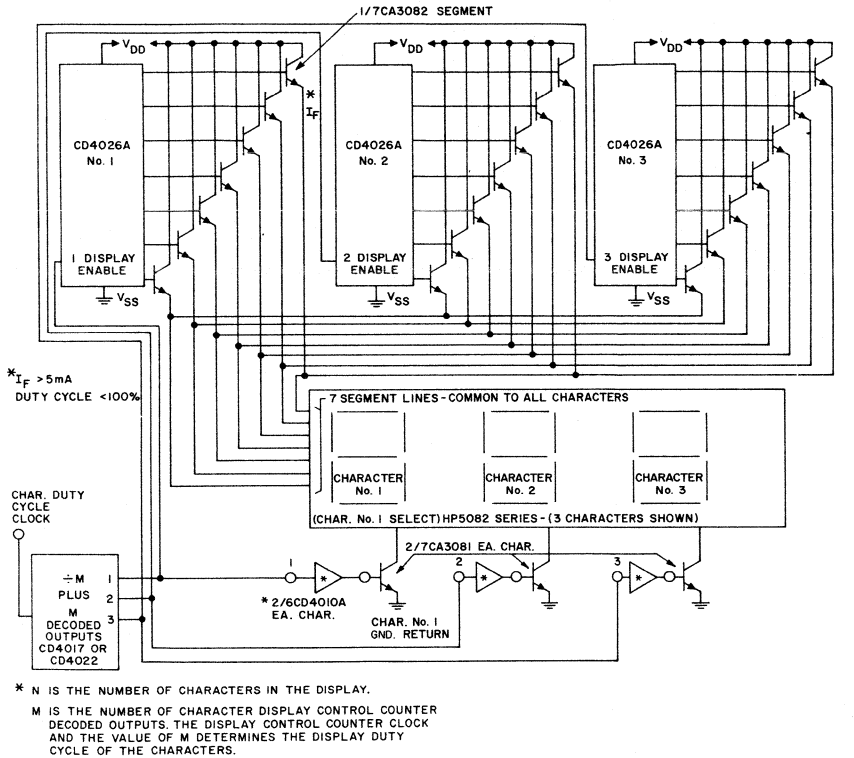


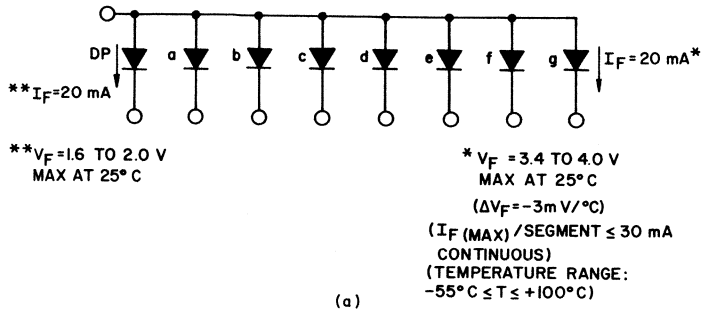
Fig.173 - Character display drive-multiplexing using the CD4026A and the HP5082 Series.

common set of CA3082 segment drivers. A common set of segment ground-return resistors would be required at the base of each CA3082.

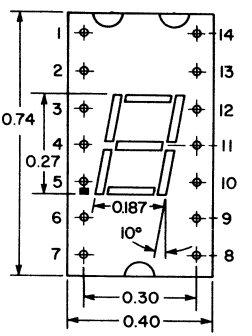
The MAN 1 is a 7-segment diffused planar GaAsP light-emitting-diode display. Fig. 174 shows the equivalent schematic diagram and physical dimensions of the MAN 1. Fig. 175 shows the brightness as a function of forward-current characteristics. Good brightness (275 foot-lamberts) is obtained at a forward current of 16 milliamperes, for a 100-per-cent duty-cycle drive mode.

Figs. 176 and 177 show the CD4033A or CD4026A being interfaced with the MAN 1 display at various supply voltages. The CD4009A (shown in Fig. 176) is able to sink 16 milliamperes or more at a logic-0 output voltage up to 2 volts, with a supply voltage (V_{DD}) of 15 volts. This feature permits a drop of 4 volts or more across the MAN 1 diodes. When the CD4009A is used in this application, care should be taken not to exceed its maximum power ratings (100 milliwatts per buffer stage; 200 milliwatts per package).

The CD4033A (shown in Fig.



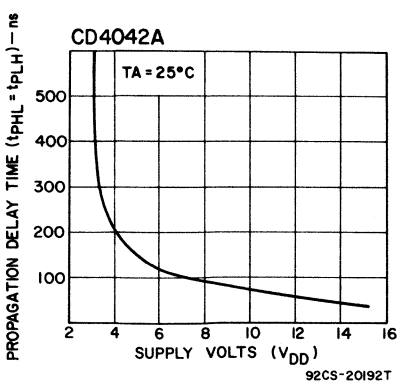
(a)



(b)

Fig. 174 - (a) Schematic diagram and (b) physical dimensions for the MAN-1.

177) provides a minimum base current of 0.4 milliamperes into the CA3081 at a supply voltage V_{DD} of 5.0 volts, for a forward current in excess of 12 milliamperes. The forward voltage of the MAN 1 (4.0 volts) limits the minimum V_{DD} to approximately 5.0 volts.



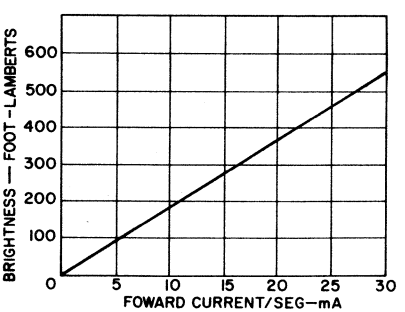


Fig. 175 - Brightness as a function of forward current for the MAN-1.

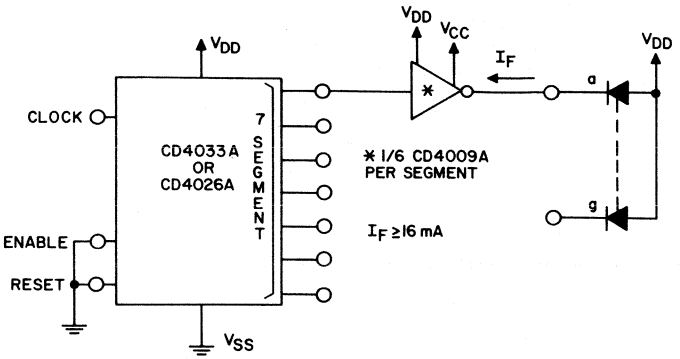


Fig.176 - CD4033A or CD4026A driving the MAN-1 at 7 volts $\leq V_{DD} \leq$ 15 volts; $V_{DD} = V_{CC}$.

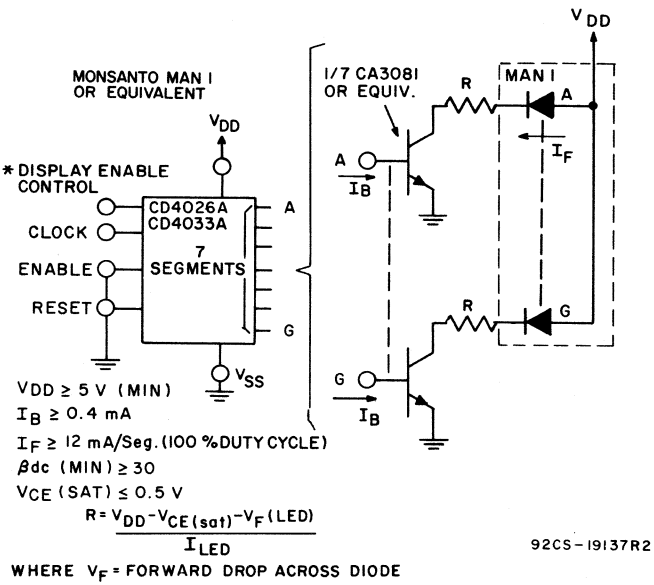


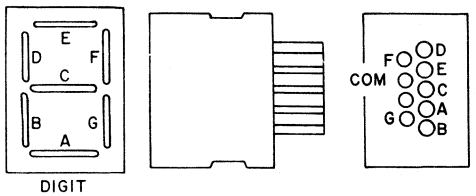
Fig.177 - CD4033A or CD4026A driving the MAN-1 at $V_{DD} \geq$ 5 volts.

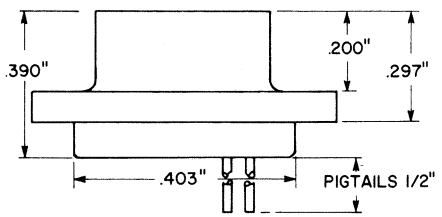
Incandescent Readouts

The Pinlite* Series "0" and "R" devices are low-power, miniaturized, incandescent readouts. Fig. 178 summarizes the voltage-current requirements and physical dimensions of these display devices. Fig. 179 shows the CD4033A being interfaced with Pinlite devices.

Fig. 180 shows the physical

*Trademark of Pinlite, Inc.





LOW-POWER INCANDESCENT READOUTS

PINLITES INC– Series O and R

TUBE REQUIREMENTS	V_T(V)	mA Segment
O-03-15	1.5	8
O-04-30	3.0	8
O-06-30	3.0	8
R-R3-20	2.0	4.3
R-R4-30	3.0	4.3

Fig. 178 - Pinlite, Inc. series "O" and "R" 7-segment display.

dimensions of RCA NUMITRON devices, DR2000, DR2100, and DR2200 series. Brightness and segment current as functions of segment voltage are shown in Fig. 181.

Fig. 182 shows the CD4033A or CD4026A being interfaced with DR2000-series displays. In the arrangement shown in Fig. 182(a), if V_{DD} is less than 8.0 volts, a CD4010A buffer must be used between the CD4033A or CD4026A segments and the CA3081. In the arrangement shown in Fig. 171(b), care should be taken not to exceed the maximum power dissipation of the CD4009A (100 milliwatts per buffer unit, 200 milliwatts per package).

Low-Voltage Vacuum Fluorescent Readouts

The TungSol Digivac S/G** Type DT1704B or DT1705D, Nippon Electric (NEC)-Type DG12E/LD915, and Sylvania Type 8894 are low-voltage and low-power vacuum fluorescent 7-segment readouts. Fig. 183 shows the physical dimensions and brightness characteristics of the TungSol Digivac DT1704B and DT1705D. A brightness level of 150 foot-lamberts (typical) is indicated at a plate voltage of 25 volts. Fig. 184 illustrates a

**Trademark of Tung-Sol Division Wagner Electric Corp.

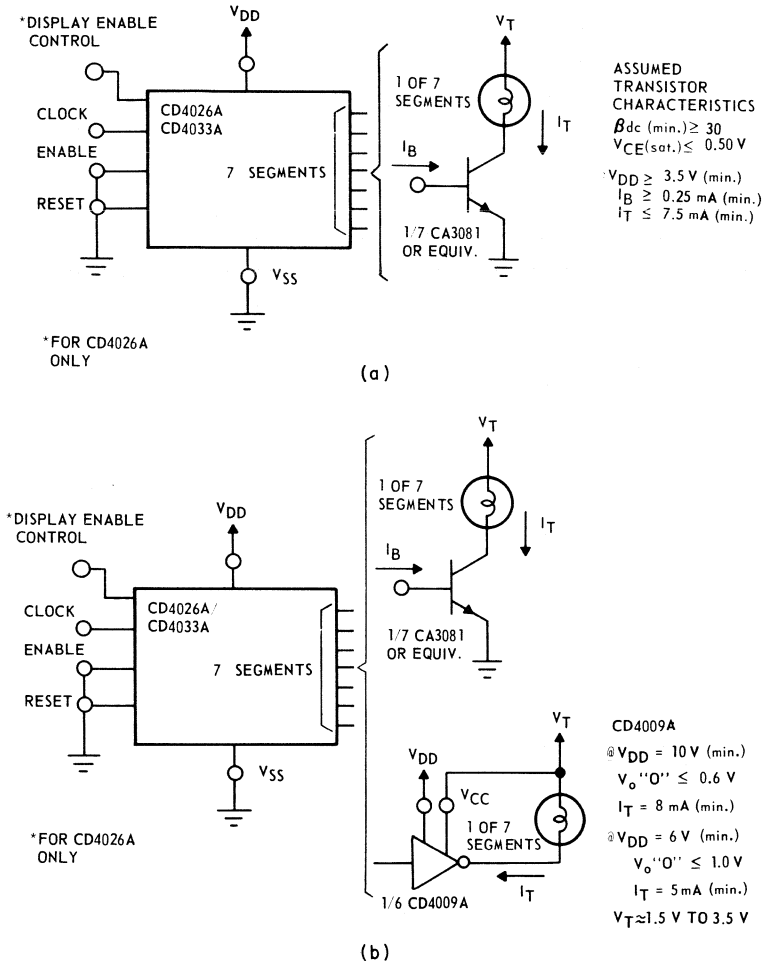


Fig.179 - Interfacing CD4033A or CD4026A with Pinlite series "0" and "R" 7-segment displays.

method of driving these devices with the CD4033A. The requirements are 100 to 300 microamperes per segment at tube voltages of 12 to 25 volts depending on the required brightness level. The filaments require 45 milliamperes at 1.6 volts, (ac or dc). With a V_{ON} of 18 volts, medium brightness in low ambient light background, will result. The point of no noticeable glow occurs at V_{OFF} = 4.5 volts.

DIGITAL TIMER/CLOCK/ WATCH APPLICATIONS

The decoded 7-segment outputs of the CD4033A can be used to

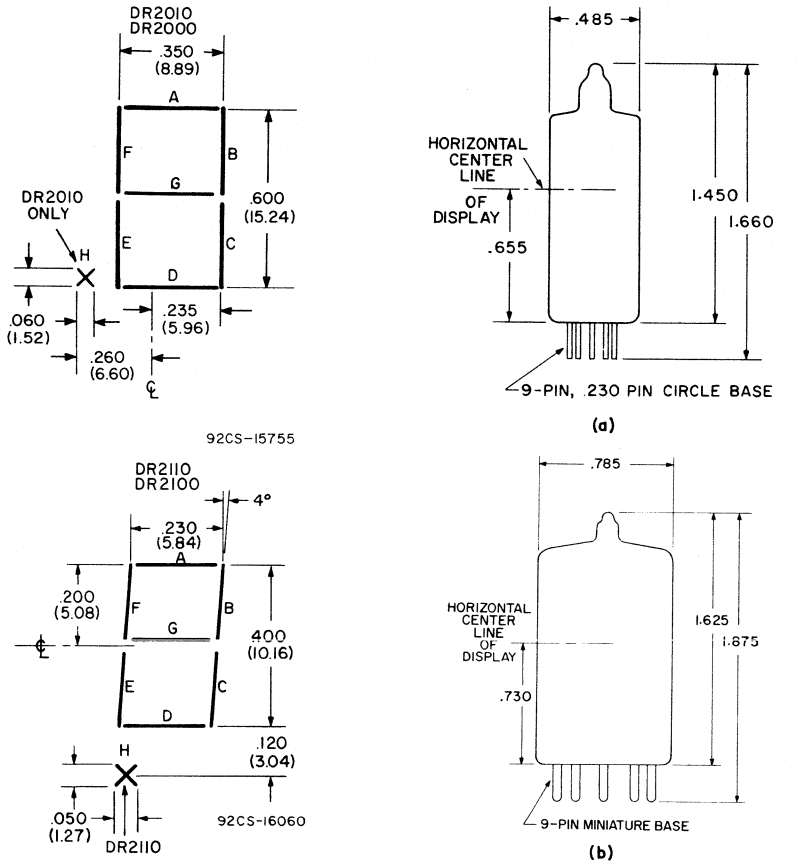


Fig.180 - Segment arrangement and physical dimensions of RCA NUMITRONS: (a) DR2000-series devices; (b) DR2100- and DR2200-series devices.

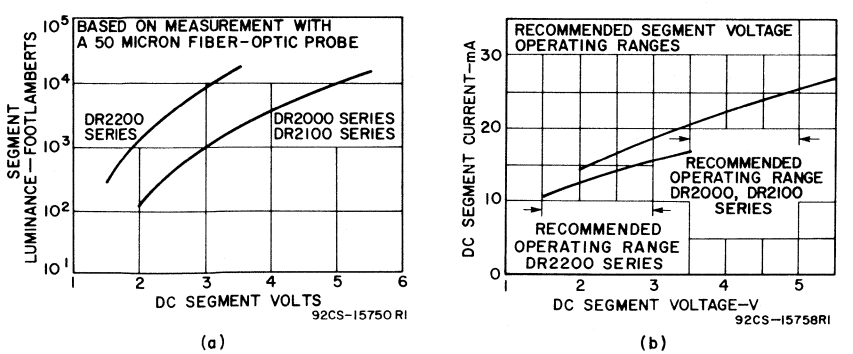


Fig.181 - (a) Brightness as a function of segment voltage and (b) segment current as a function of segment voltage for RCA NUMITRONS.

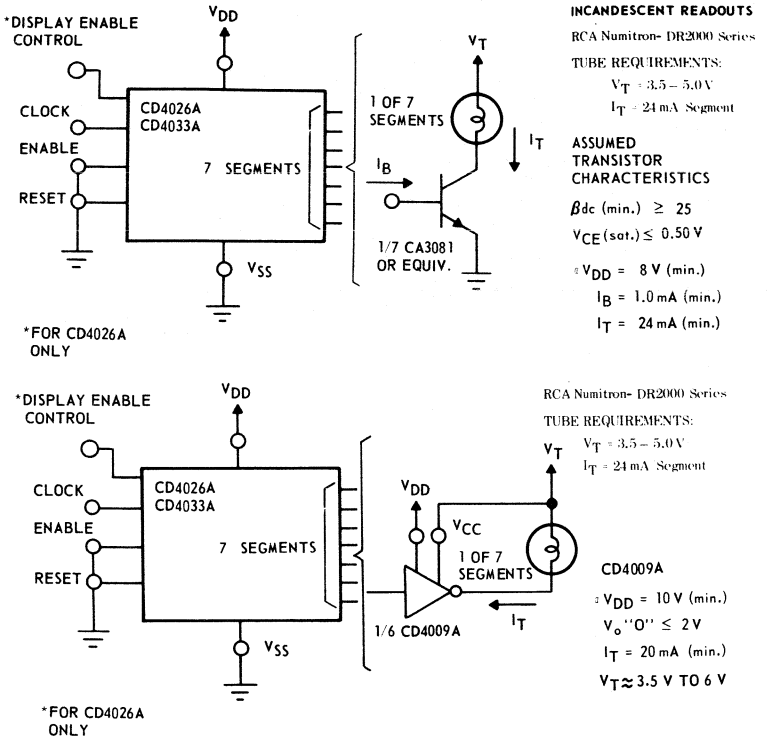
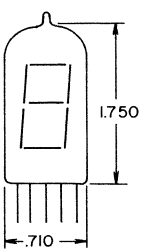


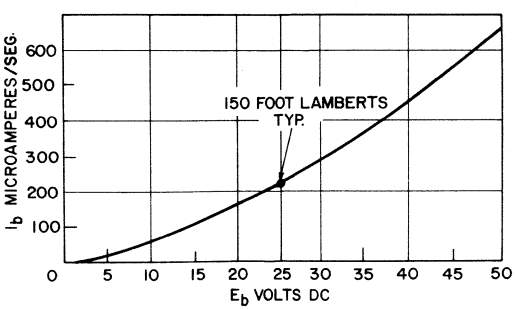
Fig. 182 - CD4033A or CD4026A driving RCA DR2000-Series NUMITRON.



TUNGSOL DIGIVAC S/G
TYPE DT1704B

NOTE: CHARACTER SIZE APPROXIMATELY:
.360" x .570" SLANTING TO THE RIGHT 8°.
SEE PUBLISHED DATA OF TUNGSOL DIVISION WAGNER ELECTRIC CORP. T438 DATED 8/69.

(a)



(b)

Fig.183 - (a) Physical dimensions and (b) plate current as a function of plate voltage for Tung-Sol S/G type DT1704B and DT1705D display devices.

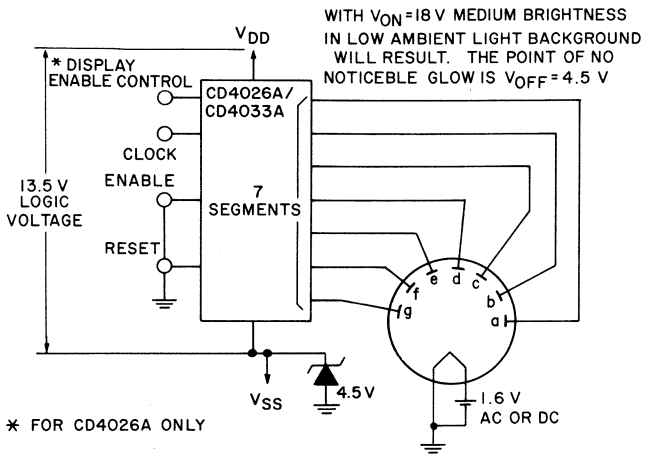


Fig.184 - Interfacing CD4033A or CD4026A with Tung-Sol S/G type DT1704B or DT1705D.

control its counting function. Table XXII shows the truth table for the CD4033A segment and carry-out signals. Fig. 185 shows the logic configurations for counting from 2 through 9 using the CD4033A signal for count control. The CD4026A can be utilized in a similar manner.

Table XXII — Truth Table — 7 Segment and Carry Out Signals

COUNTER OF:	1	2	3	4	5	6	7	8	9	10
COUNT	0	1	2	3	4	5	6	7	8	9
DECODED OUTPUT										
a	1	0	1	1	0	1	1	1	1	1
b	1	1	1	1	1	0	0	1	1	1
c	1	1	0	1	1	1	1	1	1	1
d	1	0	1	1	0	1	1	0	1	1
e	1	0	1	0	0	0	1	0	1	0
f	1	0	1	0	1	1	1	0	1	1
g	0	0	0	1	1	1	1	0	1	1
Count	1	1	1	1	1	0	0	0	0	0

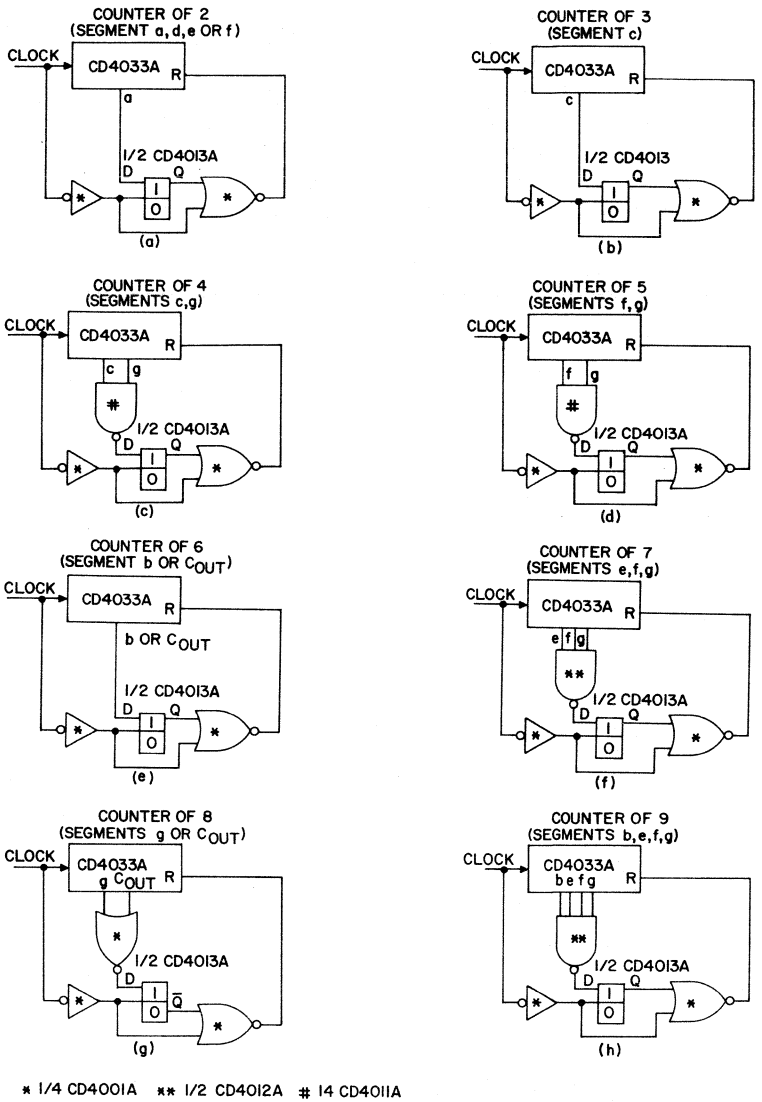


Fig.185 - Logic configurations to control counting functions of CD4033A.

Digital Display Clock/Watch Configuration (Divide-by-60, Divide-by-60, Divide-by-12)

Fig. 186 shows the logic diagram of a divide-by-60, divide-by-60, divide-by-12 digital-display counting circuit. The input clock-signal rate is 1 Hz. The two divide-by-60 counters cycle synchronously from 0 to 59, while the divide-by-12 counter cycles from 1 to 12.

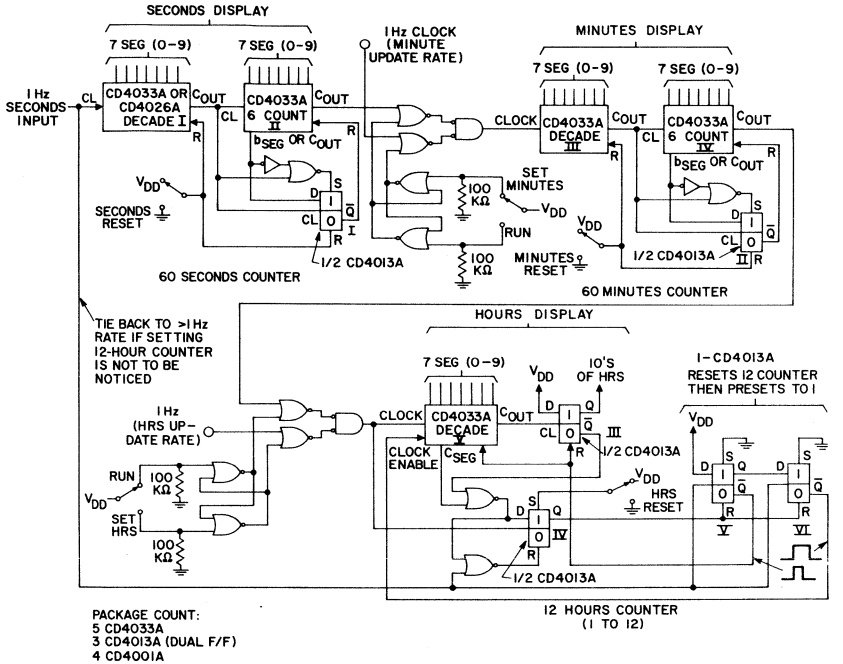


Fig. 186 - Divide-by-60, divide-by-60, divide-by-12 digital display counting circuit.

Fig. 187 shows pertinent waveforms of the divide-by-60 and divide-by-12 sections, respectively. Minutes and hours updating switches (second rate) as well as seconds, minutes, and hours reset switches are provided. A 24-hour counter can be easily substituted for the 12-hour counter.

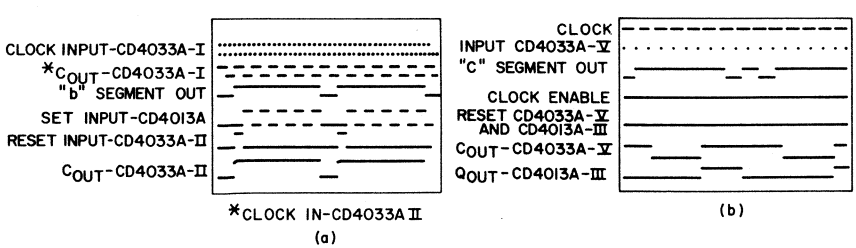


Fig. 187 - (a) Divide-by-60 voltage waveforms; (b) divide-by-12 voltage waveforms.

With reference to Figs. 186 and 187(a), the CD4033A-II b segment goes low at the 59th clock-pulse input. At the 60th clock-pulse input, the CD4033A-I goes from a 9 to a 0 and the CD4013A-I is clocked to "0" state, which in turn resets CD4033A-II from a 5 to a 0. A reset condition has been realized after 60 clock-input pulses. The CD4013A-I is then set at the 5th clock input pulse in preparation for the next cycle.

With reference to Figs. 186 and 187(b), the c segment goes low at the 12th clock input pulse. The Q output of the CA4013A-III is low from the 10th clock input pulse. At the 13th clock input pulse, CD4013A-IV is clocked to the "1" state which in turn resets CD4013A-V and VI. The CD4013A-V and VI combination then generates a one-second-wide reset pulse to the CD4033A-V and CD4013A-III reset inputs, as well as a two-second-wide pulse to the clock enable input of the CD4033A-V to advance it to the 1 count. The reset and advance-to-one operation may be clocked at a rate much faster than the seconds clock.

The CD4026A may be used in place of the CD4033A, if display blanking is desirable to effect power savings. For this case, the divide-by-12 function utilizes the ungated "c" output for counter gating.

Battery-Powered Digital Clock Prototype Using the MAN-3 LED Displays

Fig. 188 shows photographs and Fig. 189 shows the logic diagram for a prototype of a complete battery-powered digital clock that uses MAN-3 LED display devices. A 9-volt battery is used to drive all of the

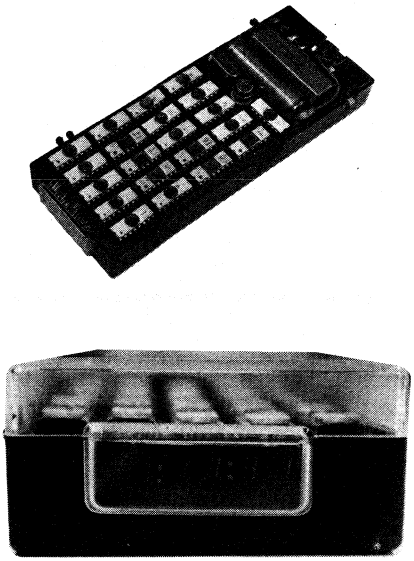


Fig. 188 - Photographs of battery-operated LED digital clock.

logic circuitry. Power drain on the 9-volt battery is approximately 7 milliamperes continuous, more than 90 per cent of which is consumed in the 262-kHz crystal-oscillator configuration. Other oscillator configurations and lower crystal frequencies permit significant reductions of this current drain. To conserve power, the MAN 3 display devices are powered by two series 1.5-volt batteries. The CD4010A's permit translation from the 9-volt logic level to the lower voltage, higher-current 3-volt display drive levels. While the display is activated, a maximum of approximately 120 milliamperes of display current is required.

Although not used in the prototype, the character-display-multiplexing methods shown in Figs. 171, 172, or 173 may be employed for greater light enhancement and/or lower power dissipation.

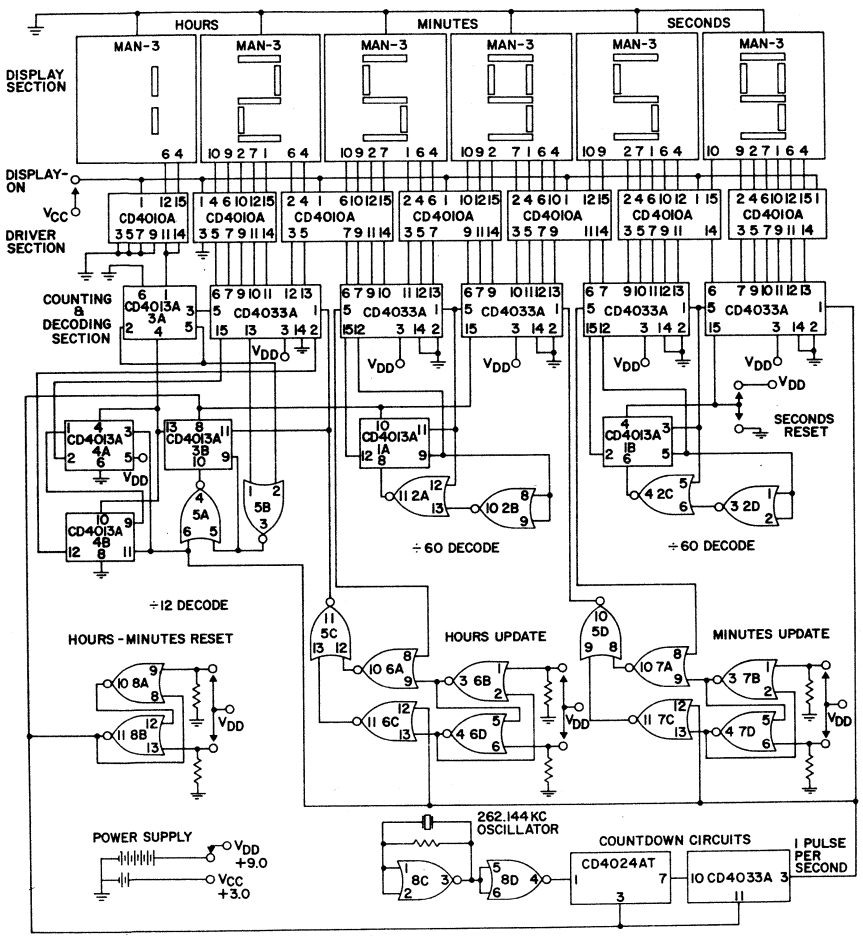


Fig. 189 - Logic/wiring Diagram for digital clock shown in Fig. 188.

Battery-Powered Digital Clock Prototype Utilizing TungSol Digivac S/G DT1704B Displays

Fig. 190 shows a photograph and Fig. 191 shows the logic diagram for a prototype of a complete battery-powered digital clock that employs TungSol Digivac display devices. As noted in the discussion of low-voltage vacuum fluorescent readouts, medium brightness levels are ob-

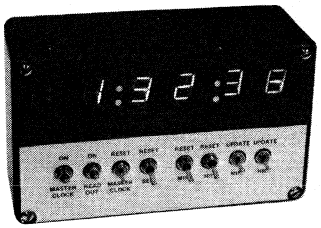


Fig.190 - Photograph of a battery-powered digital Clock that uses Digivac display devices.

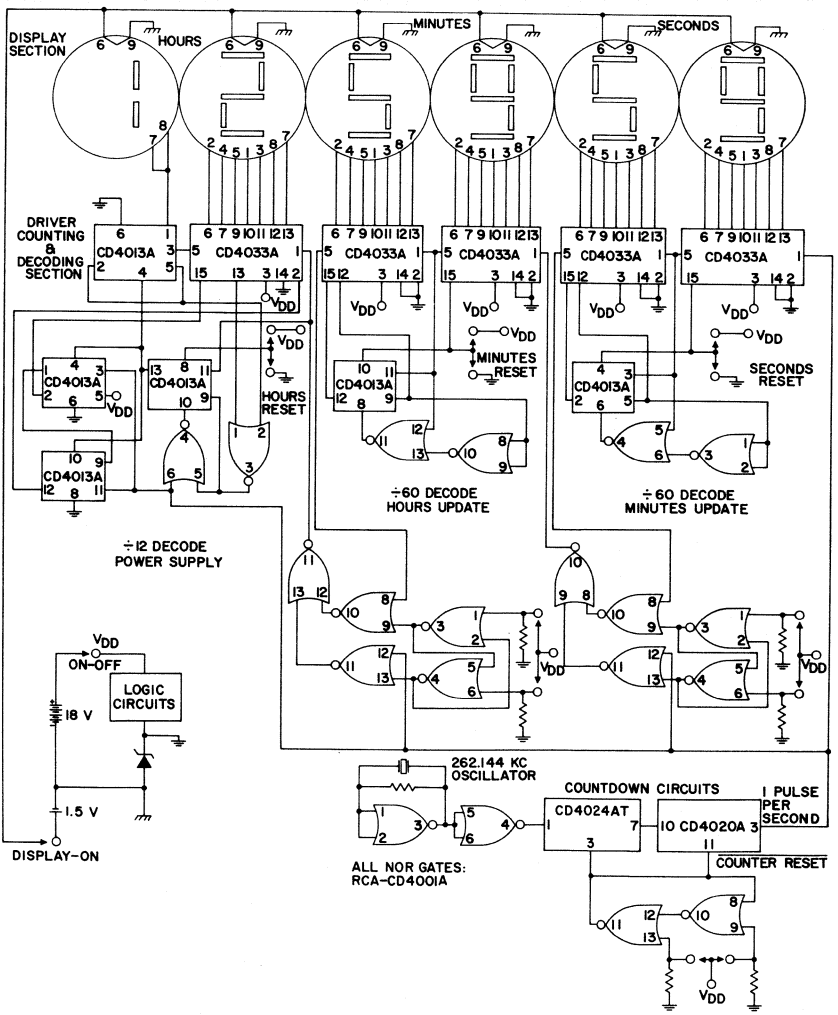


Fig.191 - Logic/Wiring Diagram for digital clock shown in Fig. 190.

tained under low to medium ambient light conditions. A larger display is achieved by use of the Digivac units than with the MAN 3 units. The logic is powered by two series 9-volt cells at V_{DD} with a 4.5-volt zener offset of V_{SS} (th effective supply voltage for the logic circuit is 18 volt -4.5 volts = 13.5 volts.) The logic circuit drives the 150-microampere segment plate currents of the Digivacs directly. The filament power for the Digivacs is supplied by two parallel 1.5-volt batteries. Filament power is off until a display is required.

DIGITAL-METER APPLICATIONS

The CD4033A and CD4026A are unique in that they have both counting and decoding on a single chip. The block diagram of Fig. 192 demonstrates the use of the CD4033A and CD4026A in digital-meter applications where time multiplexing or sampling-and-display functions are employed (to eliminate the need for holding circuits). An analog input is converted to a sequence of pulses in which the pulse count is proportional to the analog input level. Sampling rates may be fast enough to result in an apparent fixed display, or they may be slower and cause noticeable changes in display during sampling. Longer display times or display blanking during sampling may be used to prevent flicker.

Fig. 193 shows a general block diagram using the CD4033A or CD4026A in Digital Counter/Timers.

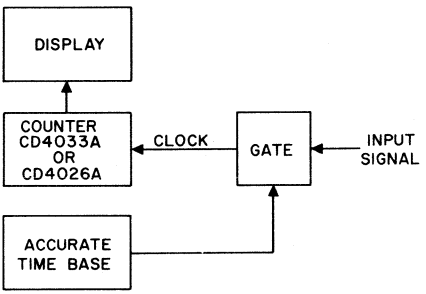


Fig. 193 - Block diagram of digital counter/timer using CD4033A or CD4026A.

As in the dc meter applications, time multiplexing of sampling and display functions is utilized.

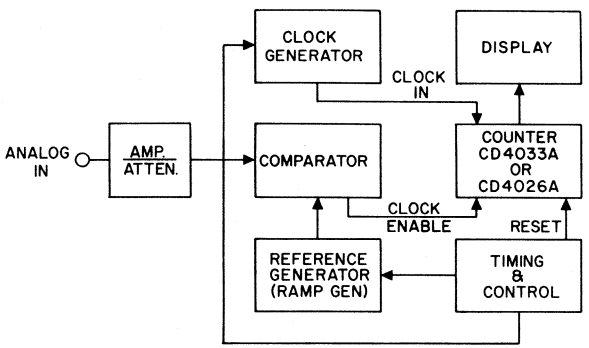


Fig.192 - Block diagram of dc meter circuit using CD4033A or CD4026A.

Digital Frequency Synthesizers

COS/MOS integrated circuits can be used in the design of low-cost, low-power digital frequency synthesizers. The synthesizer circuits that use these devices offer communications equipment designers the following advantages in comparison to comparable systems that use tuned circuits and banks of quarts crystals:

1. use of digital MSI functions to reduce cost and increase reliability;
2. use of only one crystal reference for all synthesized frequencies;
3. reduction of spurious signals and unwanted harmonics to yield a cleaner waveform by the elimination of tuned circuits (resulting in lower manufacturing-test costs and lower maintenance on equipment);
4. a simplified manual control by replacement of complex, and often unreliable, mechanical tuning mechanisms with simple digitally coded switches.

The digital frequency synthesizer uses a phase-locked loop to produce desired output frequencies dependent upon the setting of a programmable counter. The counter is controlled by dialing up frequencies with front-panel control switches. The frequency setting of the switches is always proportional to a given programmable divider ratio.

FUNDAMENTALS OF PHASE-LOCKED LOOPS

Fig. 194 shows the essential elements of a basic phase-locked loop. The output frequency of the programmable divide-by-N counter locks onto and tracks the phase of the reference frequency. A phase difference between the divide-by-N

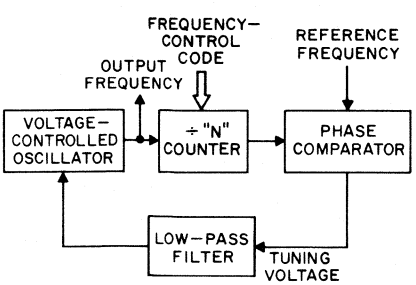


Fig. 194 - Basic digital phase-locked loop.

counter output and the reference frequency produces a correction voltage at the output of the phase comparator. The polarity of this correction voltage is such that it pulls the voltage-controlled oscillator (VCO) frequency in the right direction to cause the divide-by-N output frequency to phase-track the reference frequency. Thus, for each setting of the frequency control switches, a digital code presets the divide-by-N count to an integral number representing a desired output frequency. For each desired output frequency, there is a corresponding unique phase difference and tuning voltage. At each "tuned condition", the divide-by-N-counter output frequency is phase-locked to the reference frequency, and the two frequencies are equal.

A low-pass filter is employed in phase-locked loops to remove time-variant components from the VCO control voltage. Otherwise, for example, the reference frequency and its harmonic output from the phase detector may be of sufficient magnitude to cause an audio-rate phase jitter at the VCO output, which can result in distortion of the audio output.

PRACTICAL DIGITAL PHASE-LOCKED LOOPS

In practical digital phase-locked loops for communications systems, VCO-output frequencies are often in the vhf and uhf bands (that is, from 30 to 400 MHz). In the past, it has usually been impractical or impossible to design integrated-circuit divide-by-N counters that will operate within this range. For example, even high-power ECL circuits will not permit use of the complex divide-by-N function above 100 MHz. Low-cost techniques of reducing the VCO output frequency are required so that cost-effective low-power MSI and LSI arrays can be employed as the logical divide-by-N counter. For low-power portable communications sets, efficient COS/MOS arrays are employed using either of two basic techniques for reducing VCO output frequencies. These two techniques are prescaling and heterodyne down-conversion.

Prescaling

In the phase-locked loop shown in Fig. 195, a fixed counter prescales the VCO output frequency down by a division factor of K to the greatest value (f_K max) that can be handled by the integrated-circuit divide-by-N counter. The reference frequency (f_r) is nominally equal to the channel spacing frequency (f_c). However, when a prescaling counter is employed, the value of f_r must be reduce by a division by K. Hence,

$$f_r = \frac{f_c}{K} \qquad (18)$$

Phase-comparator reference frequencies are normally in the range of 1 to 10 kHz, while the highly stable crystal-controlled oscillators usually operate at a frequency (f_X) in the range from 2 to 5 MHz. For this reason divide-by-R counters are employed where $f_r = f_X/R$.

At phase-lock, the divide-by-N output frequency f_n tracks the reference frequency f_r; therefore, $f_n = f_r$. Furthermore, the modulo (N) of

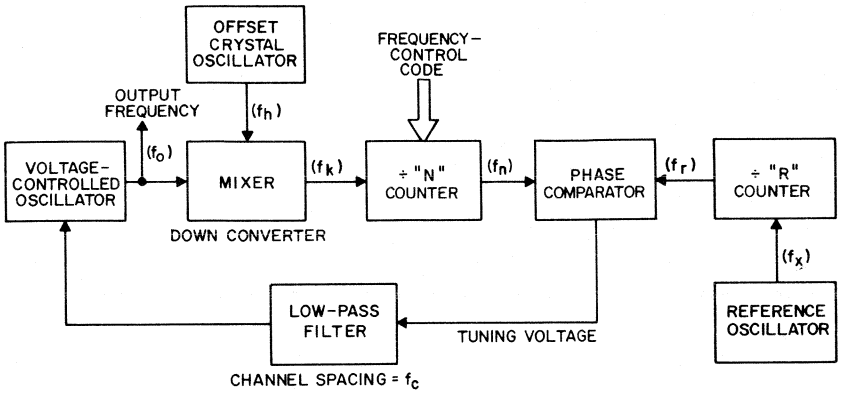


Fig. 195 - Digital phase-locked loop with prescaler.

the divide-by-N counter uniquely determines the output frequency (f_O) that will satisfy the following equation:

$$f_O = f_n(K)N. \qquad (19)$$

K operates in a fixed-integer counter, and N operates in a programmable modulo-N counter in which the modulo is programmed by an external frequency-control code. The range of N is given by

$$N\ max = \frac{f_O\ max}{f_C}, \qquad (20)$$

and

$$N\ min = \frac{f_O\ min}{f_C} \qquad (21)$$

For specified values of K, N, R, f_X, f_O, and f_C, it is simple arithmetic to specify completely all digital functions including the phase comparator, which, in most cases, also functions digitally. Further, the divide-by-N counter can be broken into decade or binary segments. This approach leads directly to specification of programmable-switch design. The low-pass filter can then be specified for optimum rejection of reference-frequency components.

However, because the frequencies of signals within the loop shown in Fig. 195 vary over a range of N, optimum stabilization of the negative part of the loop is compromised by the variation of gain with frequency. In addition to loop stabilization, the designer must also consider several other aspects of phase-locked loops, including the following items:

1. loop settling time and switching time,
2. resolution (which is related to reference-oscillator accuracy),
3. spectral purity (spurious outputs and signal-to-phase-noise ratio).
4. loop modulation (practical mode for transceivers),
5. sweep mode (applicable to test-equipment usage),
6. system interface (remote code programming and preset channel memory).

Heterodyne Down-Conversion

Fig. 196 illustrates a digital phase-locked loop that uses heterodyne down-conversion. In this type of loop, the input frequency to the divide-by-N counter (f_k) is described as follows:

$$f_k = f_o - f_h. \qquad (22)$$

An offset crystal oscillator is employed to "mix down" the VCO output frequency (f_o), and the desired output frequency range of f_k is enclosed by suitable band-pass filtering. In the scheme shown in Fig. 196, the output frequency is expressed as:

$$f_o = f_n N. \qquad (23)$$

The input frequency to the N counter is given by

$$f_k = f_o - f_h. \qquad (24)$$

The range of the N counter is defined by the following two equations:

$$N\ max = \frac{f_k\ max.}{f_c} \qquad (25)$$

$$N\ min = \frac{f_k\ min.}{f_c} \qquad (26)$$

In many synthesizer systems that employ heterodyne down-conversion, more than one value of offset frequency (f_h) is switched in. For example, if the desired VCO output frequency band is broken into two equal ranges, and if values of f_h are switched in for the two respective bands, the range of N is exactly half that used in a prescaling system. The range of N is traversed twice in tuning across the entire band. Practical application of this method is explained in the subsequent discussion of an FM-broadcast-band synthesizer.

In comparison to the prescaling technique, heterodyne down-conversion offers two significant advantages. First, the reference frequency f_r is equal to the channel spacing f_c; as a result, the loop band pass is wider. Second, the power consumption is lower; the offset

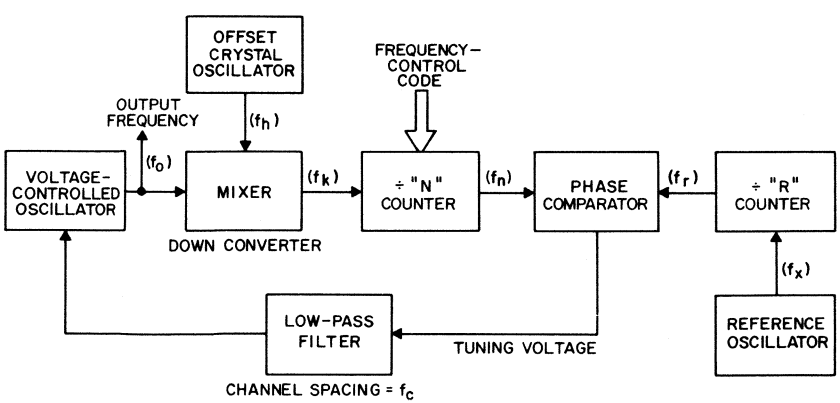


Fig. 196 - Digital phase-locked loop with heterodyne down-converter.

oscillator and mixer, therefore, can be extremely efficient.

The disadvantage of the heterodyne technique is that the use of a second reference crystal and a mixer may introduce spurious beat and sum frequencies.

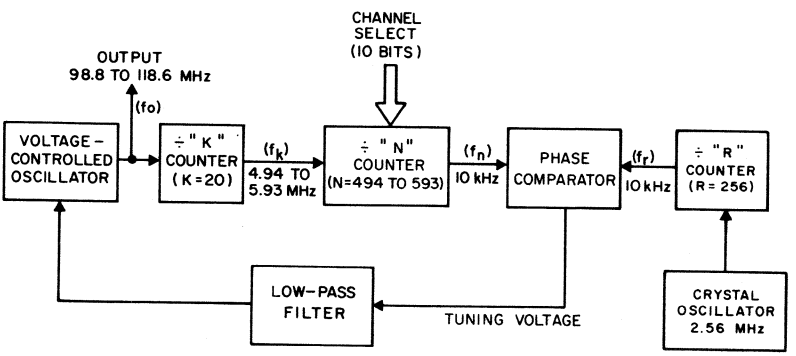
F/M RECEIVER SYNTHESIZERS

FM-broadcast-receiver synthesizers, either prescaling or down-conversion types, can be designed to use efficient COS/MOS integrated circuits as principal counter elements. One-hundred FM channels are spaced 200 kHz apart in the 88-to-108-MHz band. The channel-1 carrier frequency is 88.1 MHz; channel 100 is 107.9 MHz. Because the standard FM if frequency is centered at 10.7 MHz, the synthesizer must provide high-side local-oscillator output frequencies of 98.8 to 118.6 MHz.

Prescaler System

FM synthesizer design parameters can be calculated and plugged into the block diagram shown in Fig. 195. The resulting synthesizer block diagram and parameter calculations are illustrated in Fig. 197.

Divide-by-N Counter – The divide-by-N counter is parallel loaded to have a unique count (modulus) for each required synthesizer output-channel frequency. Each counter step represents a 200-kHz channel. For example, as shown in Fig. 197, to tune the system to 118.6 MHz, a



f_c (CHANNEL SPACING) = 200 kHz

$k = 20$

$f_k = \frac{f_o}{20}$: f_k MAX. = $\frac{118.6\ \text{MHz}}{20} = 5.93\ \text{MHz}$, f_k MIN. = $\frac{98.8\ \text{MHz}}{20} = 4.94\ \text{MHz}$

$f_r = \frac{200\ \text{kHz}}{20} = 10\ \text{kHz}$

N MAX. = $\frac{118.6\ \text{MHz}}{200\ \text{kHz}} = 593$

N MIN. = $\frac{98.8\ \text{MHz}}{200\ \text{kHz}} = 494$

$R = \frac{2.56\ \text{MHz}}{10\ \text{kHz}} = 256$

Fig. 197 - FM-band synthesizer using prescaler.

count of 593 is loaded into the counter, and "divide-by-593" results. The N counter should be considered as counting down repeatedly from 593 to zero. Fig. 198 illustrates the counter organization. For each frequency integer, there is a one-to-one relation between each switch (one frequency integer) and the corresponding counter block.

For example, a divide-by-5 counter programs the 200-kHz integer. Five counts of this counter step the 1-MHz counter by a "1" count.

Although the span of the N counter must be 494 to 593, as illustrated in Fig. 197, the actual range of a practical N-counter for an FM-band digital synthesizer can be offset as indicated in Table XXIII. In this case, six counts (equivalent to a 1.2-MHz offset) are added to both the top and bottom of the counter range to make the actual count span from 500 to 599; two simplifications in the synthesizer design result from this refinement. First, the 100-MHz binary count shown in Fig. 198 always starts in the 100-MHz state; therefore, it does not have to be under switch control. Second, the necessary one-to-one correspondence between switch position and N-count present state can be achieved. That is, when switching from channel 5 to channel 6, as shown in Table XXIII, the system is in fact switching from the 88.9-MHz channel to the 89.1-MHz channel. It should be noted that the two least significant integers switch over and that, as the actual local-oscillator injection frequency goes from 99.6 MHz to 99.8 MHz, only one integer switches over. However, the 1.2-MHz-offset frequencies of 100.8 and 101.0 MHz do switch over in the two least signi-

Table XXIII – Divide-by-N Counter/Frequency Relationships

CHANNEL NO.	FM RECEIVER FREQUENCY (fm) MHz	LO INJECTION FREQUENCY (f_o) (f_o = fm + 10.7) MHz	REQUIRED N COUNT	OFFSET FREQUENCY (f_o + 1.2 MHz) MHz	OFFSET N-COUNT (N + 6)
1	88.1	98.8	494	100.0	500
2	88.3	99.0	495	100.2	501
3	88.5	99.2	496	100.4	502
4	88.7	99.4	497	100.6	503
5	88.9	99.6	498	100.8	504
6	89.1	99.8	499	101.0	505
⋮	⋮	⋮	⋮	⋮	⋮
98	107.5	118.2	591	119.4	597
99	107.7	118.4	592	119.6	598
100	107.9	118.6	593	119.8	599

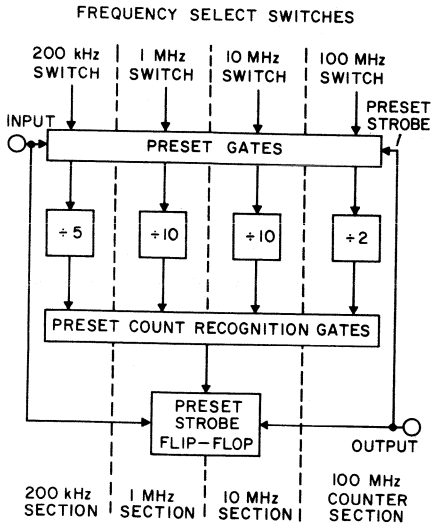


Fig. 198 - Organization of divide-by-N counter.

ficant integers. Therefore, the 1.2-MHz offset makes it possible to use the needed switch-compatible N counter.

Fig. 199 shows a logic diagram for the four counting elements of the N counter illustrated in Fig. 197. Table XXIV contains the counter truth tables, and Fig. 200 is a detailed logic diagram of the divide-by-5 counter. Table XXV illustrates that the 9-bit frequency-select code permits presetting the N counter to counts ranging from 500 to 599. The counter "down-counts" to the "8" state, at which time a preset strobe count-recognition signal goes high (output of G2 of Fig. 199).

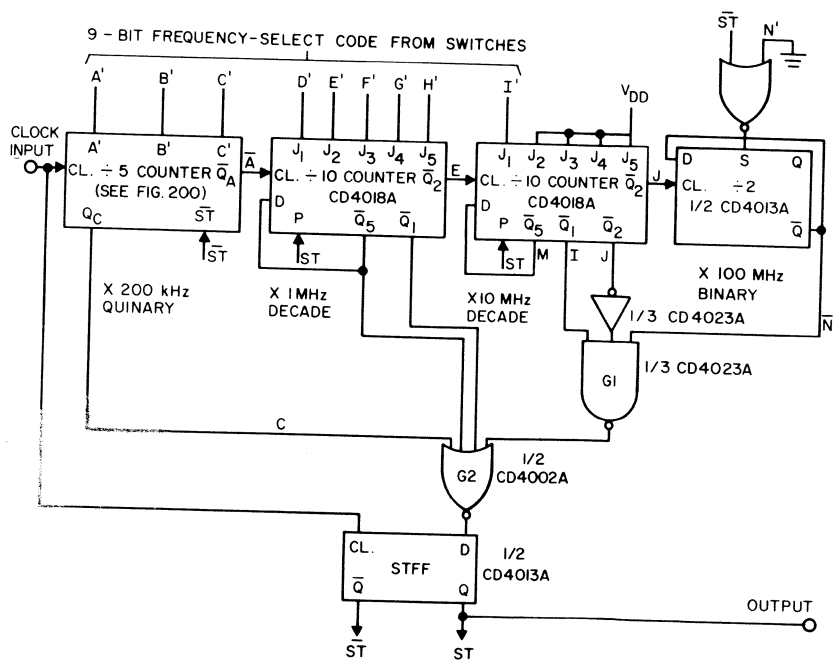


Fig.199 - Logic diagram for the divide-by-N counter.

Table XXIV – Divide-By-N Counter Truth Tables

(a) Divide-by-5 Counter		(b) Divide-by-10 Counter		(c) Divide-by-2 Counter	
X200 kHz	A B C	X1MHz / X10MHz	D E F G H / I J K L M	X100 MHz	N
4	0 1 1	9	0 0 1 1 1	1	1
3	0 0 0	8	0 0 0 1 1	0	0
2	1 0 0	7	0 0 0 0 1		
1	1 1 0	6	0 0 0 0 0		
0	1 1 1	5	1 0 0 0 0		
		4	1 1 0 0 0		
		3	1 1 1 0 0		
		2	1 1 1 1 0		
		1	1 1 1 1 1		
		0	0 1 1 1 1		

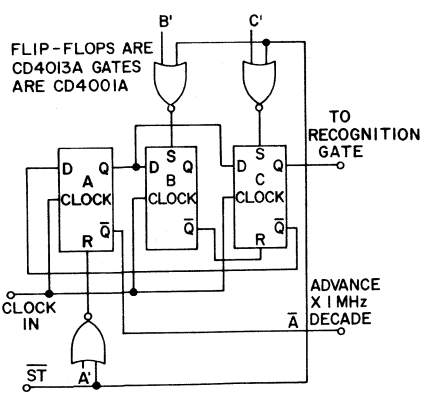


Fig. 200 - Logic diagram for divide-by-5 counter.

Fig. 201 shows the critical preset strobe-generation timing sequence. Following the "high" that appears on D of STFF (Fig. 199), the strobe goes high on the next positive clock transition as shown in Fig. 201. The strobe presets the entire N counter to the dialed frequency. The immediately succeeding positive clock transition is lost as a result of its being overlapped by the preset strobe. The second following clock transition, however, trips the counter to state N-1. Table XXVI is a wiring truth table for two frequency-select switches, S_1 and S_2. The nine wires A' through I' follow the patterns indicated and interface directly with the divide-by-N counter of Fig. 199.

Divide-by-N-Counter Implementation – The divide-by-N counter is the frequency-control element of the digital phase-locked loop. It is logically complex and must operate at the highest possible frequency consistent with minimum power for battery operation. The COS/MOS low-voltage technology exhibts several characteristics that allow out-

Table XXV – Divide-By-"N" Counter Recognition-State Truth Table

	TRUTH TABLE CODE													
COUNT	A	B	C	D	E	F	G	H	I	J	K	L	M	N
599	0	1	1	0	0	1	1	1	1	1	1	1	1	1
598	0	0	0	0	0	1	1	1	1	1	1	1	1	1
597	1	0	0	0	0	1	1	1	1	1	1	1	1	1
501	1	1	0	0	1	1	1	1	0	1	1	1	1	1
500	1	1	1	0	1	1	1	1	0	1	1	1	1	1
499	0	1	1	0	0	1	1	1	0	0	1	1	1	0
10	1	1	1	1	1	1	1	0	0	1	1	1	1	0
9	0	1	1	1	1	1	1	1						
8	0	0	0	1	1	1	1	1						
7	1	0	0	1	1	1	1	1						
6	1	1	0	1	1	1	1	1						
5	1	1	1	1	1	1	1	1						
4	0	1	1	0	1	1	1	1						
3	0	0	0	0	1	1	1	1						
2	1	0	0	0	1	1	1	1						
1	1	1	0	0	1	1	1	1						
0	1	1	1	0	1	1	1	1						

$N_{max.} \equiv 599 - 6 = 593$

$N_{min} \equiv 500 - 6 = 494$

Recognition State
Generate Preset Strobe
Effective "O" State

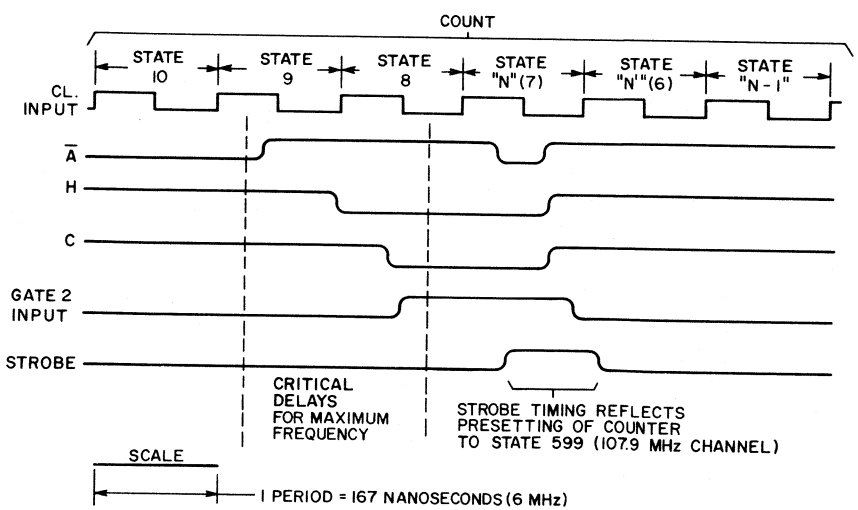


Fig.201 - Divide-by-N preset-state timing.

Table XXVI – Frequency-Select Switch Table

S1 (kHz)					S2 (MHz)							
RECEIVER FREQUENCY kHz	POS.	WIRES A'	B'	C'	RECEIVER FREQUENCY MHz	POS.	WIRES D'	E'	F'	G'	H'	I'
900	5	0	0	0	107	20	0	0	1	1	1	1
700	4	0	1	1	106	19	0	0	0	1	1	1
500	3	1	1	1	105	18	0	0	0	0	1	1
300	2	1	0	1	104	17	0	0	0	0	0	1
100	1	1	1	0	103	16	1	0	0	0	0	1
					102	15	1	1	0	0	0	1
					101	14	1	1	1	0	0	1
					100	13	1	1	1	1	0	1
					99	12	1	1	1	1	1	1
					98	11	0	1	1	1	1	1
					97	10	0	0	1	1	1	0
					96	9	0	0	0	1	1	0
					95	8	0	0	0	0	1	0
					94	7	0	0	0	0	0	0
					93	6	1	0	0	0	0	0
					92	5	1	1	0	0	0	0
					91	4	1	1	1	0	0	0
					90	3	1	1	1	1	0	0
					89	2	1	1	1	1	1	0
					88	1	0	1	1	1	1	0

Note:
"0" ≡ GROUND
"1" ≡ V_{DD}

standing devide-by-N counter performance.

Figs. 199 and 200 show COS/MOS counter logic containing the following complement of eight low-voltage devices.

1	CD4023A Triple 3-Input NAND Gate
1	CD4001A Quad 2-input NOR Gate
1/2	CD402A Dual 4-input NOR Gate
3	CD4013A Dual "D" Flip-Flop
2	CD4018A Presettable Decade Counter

Characteristics of the above devices are contained in RCA data sheet File No. 479. This family of low-voltage devices (3 volts to 15 volts) exhibits a typical flip-flop toggle rate (maximum clock input frequency) of 10 MHz at 10 volts and a typical gate delay of 25 nanoseconds at 10 volts. In both cases, a fan-out of 3 (15 picofarads) is used.

Before examining the performance of the N counter, some additional operating details are of interest. The four counter sections shown in Fig. 199 are rippled; that is, they are not synchronously clocked.

As a result, speed and, therefore, COS/MOS power are substantially less in each succeeding counter section from left to right; the divide-by-2 counter, for example, operates at one five-hundredth of the input-clock rate.

Briefly, counter operation is as follows:

(1) The synchronous divide-by-5 counter (Fig. 200) advances the 1-MHz decade counter once every five counts; that is, when A goes from 1 to 0 as shown in Table XXIV(a).

(2) The synchronous 1-MHz decade counter advances the 10-MHz decade once every 50 counts; that is, when E goes from 1 to 0 as shown in Table XXIV(b).

(3) The 10-MHz decade advances the 100-MHz binary counter once every 500 counts, that is, when J goes from 1 to 0.

(4) Preset count-logic-state-recognition occurs at count 8, as shown in Table XXIV.

(5) Preset strobe generation occurs at count 7, as shown in Fig. 201.

The CD4018A decade counter, which is a 5-stage Johnson-counter configuration, has two outstanding characteristics. First, each flip-flop changes state at one-tenth of the input rate; hence, the power/speed ratio is minimized. Second, frequency-control switching is accomplished by use of a single-wafer Johnson-code switch. A simple miniaturized 2-pole 10-position switch, such as that shown in Fig. 202, may be used.

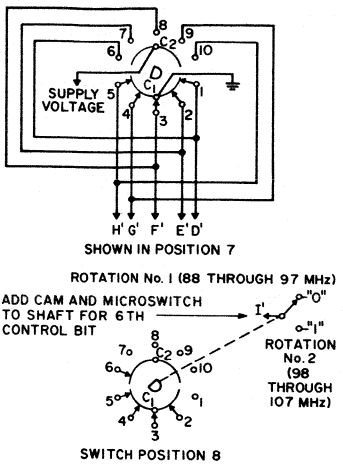


Fig. 202 - Frequency control switch S2 (Ref. Table XXVI).

Divide-by-N-Counter Performance – Fig. 203 shows the power consumption of the divide-by-N counter as a function of operating frequency with a V_{DD} of 15 volts. The curves show that a frequency of 8.7 MHz is possible. Maximum operating frequencies for 10 volts and 5 volts are 6.2 MHz and 2.7 MHz, respectively. The maximum operating

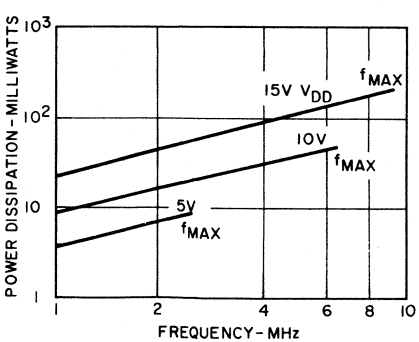


Fig. 203 - Power consumption of the divide-by-N counter.

frequency required by the circuit shown in Fig. 197 is 5.93 MHz, which can be obtained with a supply potential of 9.6 volts and with a power consumption of 47 milliwatts.

Operation of the divide-by-N counter using only a 3-volt power supply is possible. In such a case, the maximum operating frequency is 55 kHz, and the power consumption is only 40 microwatts.

Fig. 204 illustrates the decrease in maximum operating frequency as the temperature is increased. This

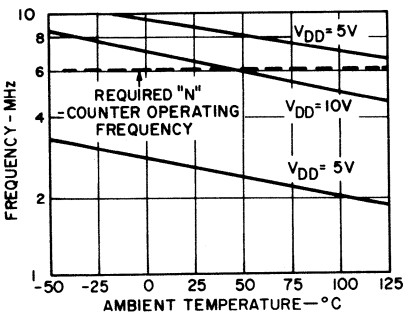


Fig. 204 - Temperature-frequency characteristics of divide-by-N counter.

curve shows that 5.93-MHz operation can be achieved up to 50°C at a supply potential of 10 volts. The dynamic signal power remains fairly constant from −25°C to more than +100°C, with variations well within 10 per cent of the power dissipated at 50°C, as shown in Fig. 205.

For 6-MHz operation at 10 volts, the critical timing waveforms for generation of the preset strobe are shown in Fig. 206. Delay from the positive edge of the clock pulse of count 9 (Fig. 201) to the output of gate 2 (Fig. 199) is 250 nanoseconds. Maximum allowable delay is 320 nanoseconds, or nearly two clock periods at 6 MHz. Thus a safe-

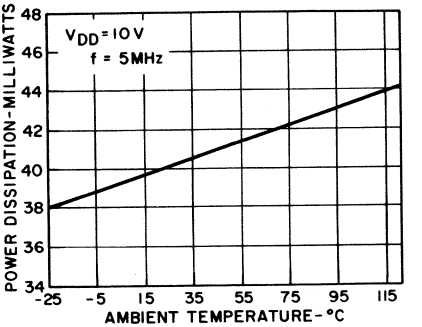


Fig. 205 - Dynamic power dissipation of divide-by-N counter.

operation margin of 60 nanoseconds exists.

The complementary nature of the COS/MOS devices permits a wide range of operating voltages to be

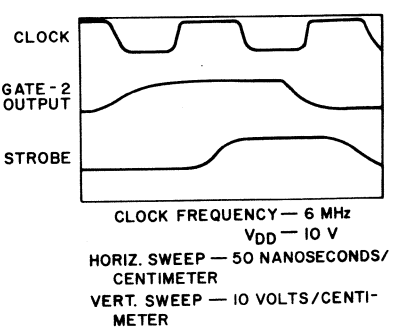


Fig.206 - Strobe generation timing.

used and yields high noise immunity. Fig. 207 shows that 6-MHz operation can be achieved using a 12-volt supply having 2.3 volts peak-to-peak ripple.

Quiescent power dissipated by any COS/MOS logic system is extremely low. The quiescent power dissipated at +25°C by the N counter of Fig. 199 is 2 microwatts at a V_{DD}

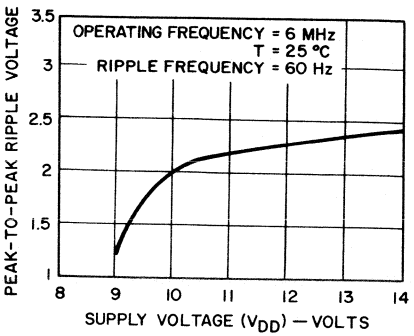


Fig. 207 - Ripple-frequency characteristics of Divide-by-N counter.

of 10 volts. Fig. 208 shows the increase in quiescent power with increasing temperature. For the system described, however, the quiescent power figure is academic because the N counter runs continuously. Some ultra-low-power digital frequency-synthesizer systems place the N counter and other loop elements on standby power periodically.

The power consumption of the COS/MOS divide-by-N counter is substantially less than that of a bipolar divide-by-N counter performing the identical function. The popular 54N TTL logic, or the equivalent, is normally used for high-speed counting, as shown in Fig. 16, and 54L logic, or the equivalent, is used for lower-speed functions.

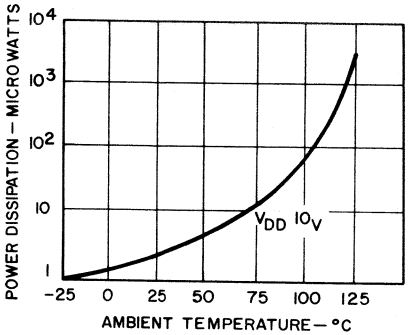


Fig. 208 - Quiescent power dissipation of divide-by-N counter.

Approximately 265 milliwatts at +5 volts is required by the bipolar design of Fig. 209, compared with only 50 milliwatts for the COS/MOS design at a V_{DD} of 10 volts.

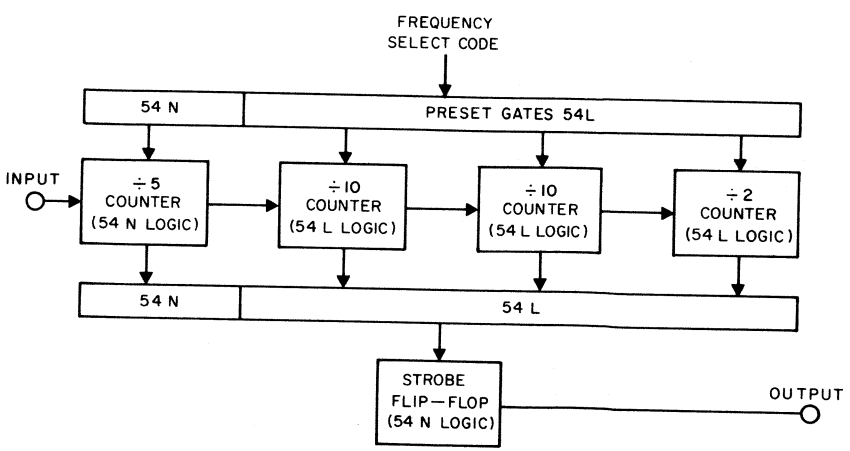


Fig.209 - Bipolar-logic divide-by-N counter.

Divide-by-R Counter – The FM receiver synthesizer system shown in Fig. 197 requires a fixed reference counter to divide by 256. To accomplish this function, a 2.56-MHz reference crystal oscillator is counted down to the 10-kHz phase-comparison frequency. One CD4020A 14-stage ripple-carry counter may be used for this purpose. Fig. 210 shows power consumption as a function of supply voltage for this counter. For a V_{DD} of 5 volts, power is below 3 milliwatts for the 2.56-MHz input.

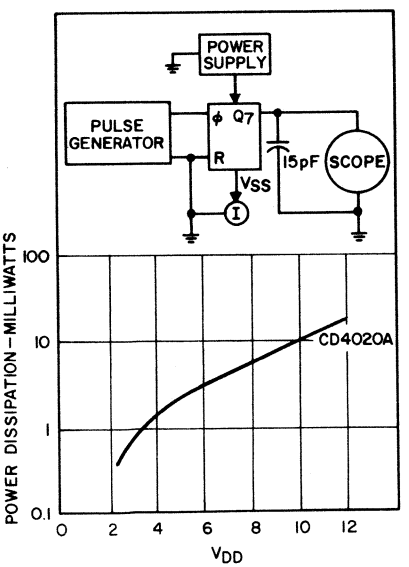


Fig. 210 - Power consumption of divide-by-R counter.

Phase-Comparator – A simple type "D" flip-flop (COS/MOS CD4013A) will suffice for a phase comparator in the digital phase-locked loop system of Fig. 197. Fig. 211

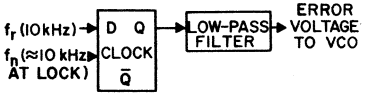


Fig.211 - Flip-flop phase comparator.

shows the simple flip-flop phase comparator and low-pass filter; Fig. 212 demonstrates the operation of this phase comparator. A positive charge is impressed on the low-pass filter when f_n is greater than f_r in the case shown. Also, phase-lock can occur only during 180° of the period. In the case shown in Fig. 212, negative feedback in the loop exists during the 180° when f_r is positive. When f_n coincides with the negative half-phase of f_r, positive feedback exists

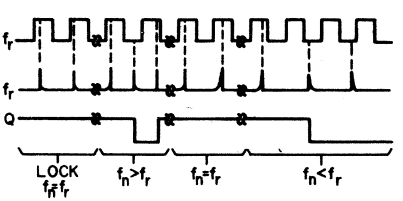


Fig. 212 - Operating waveforms for flip-flop phase comparator.

in the loop, and lock-up cannot occur. The waveforms of Fig. 212 show that when f_n is equal to f_r lock-up exists, and that when f_n is not equal to f_r either an out-of-lock condition exists or an error-correction voltage is being produced during lock-up.

The simple COS/MOS flip-flop phase comparator of Fig. 211 consumes only 0.1 milliwatt at a V_{DD} of 10 volts. Although only one flip-flop is required, a bulky LC filter must be provided to smooth and store the

output error voltage. Also, such a phase comparator is non-centering; when loss of an input signal occurs, a maximum error voltage is created.

Another example of a COS/MOS low-power phase comparator is the familiar Exclusive-OR gate (CD4030A). The primary advantage of this unit is that it produces an error voltage for frequency centering when one of the inputs is lost.

Another high-performance phase comparator is a sample-and-hold circuit employing COS/MOS, as shown in Fig. 213. The sample-and-hold phase comparator substantially reduces the 10-kHz carrier frequencies, and thus reduces filter requirements for the loop and increases the loop gain-bandwidth product. COS/MOS integrated circuits are used as the ramp generator and the sampling switch, as illustrated in Fig. 213. Total power consumption at 10-kHz operation is less than 15 milliwatts.

Crystal Oscillator – The required 2.56-MHz crystal oscillator can be implemented with a COS/MOS inverter-amplifier and feedback network, as shown in Fig. 214. The inverter is one-third of a CD4007A integrated circuit. Power consumption is approximately 2 milliwatts at a V_{DD} of 5 volts.

Down-Conversion System

From the previous discussion of the prescaling FM receiver synthesizer, it is apparent that the system consumes relatively large amounts of power. The system shown in Fig. 196, however, illustrates a heterodyne down-conversion technique that avoids high-frequency digital prescaling. Fig. 215 shows a detailed block diagram of a down-conversion system in which a divide-by-2 prescaler is also employed to simplify the design.

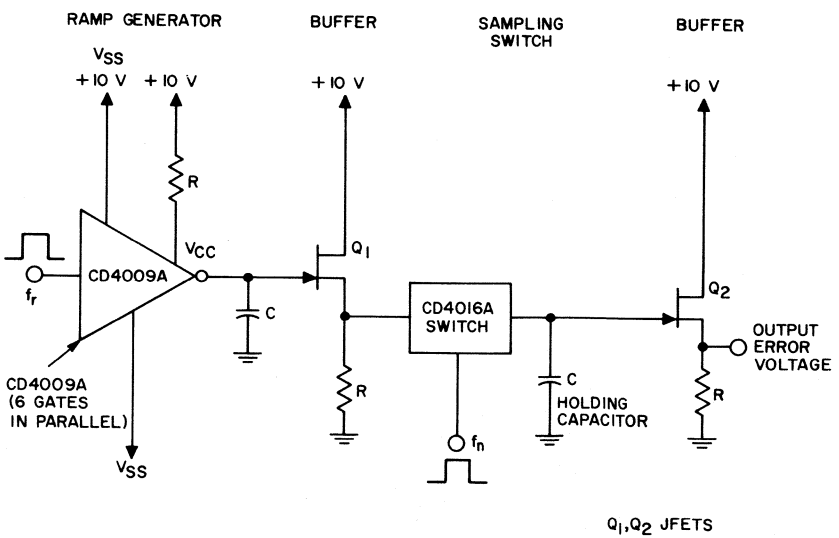


Fig.213 - Sample-and-hold phase comparator.

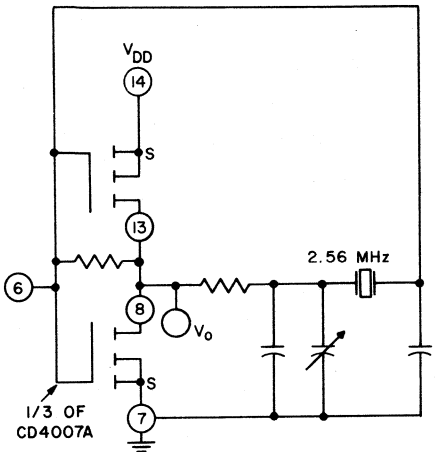


Fig.214 - Crystal oscillator.

Table XXVII shows how the heterodyne down-conversion operates. For frequencies selected between 88.1 MHz and 97.9 MHz, the respective local-oscillation frequencies of 98.8 MHz and 108.6 MHz are down-converted by 98 MHz to 0.8 MHz and 10.8 Mhz respectively. The range between those two frequencies is then prescaled by 2 down to 0.4 MHz and 5.4 MHz, which is the range of operating frequencies for the divide-by-N counter. For the divide-by-N counter of Fig. 215, the range is determined as follows:

$$\text{N max.} = \frac{10.8\ \text{MHz}}{0.2\ \text{MHz}} = 54, \qquad (27)$$

$$\text{N min.} = \frac{0.8\ \text{MHz}}{0.2\ \text{MHz}} = 4. \qquad (28)$$

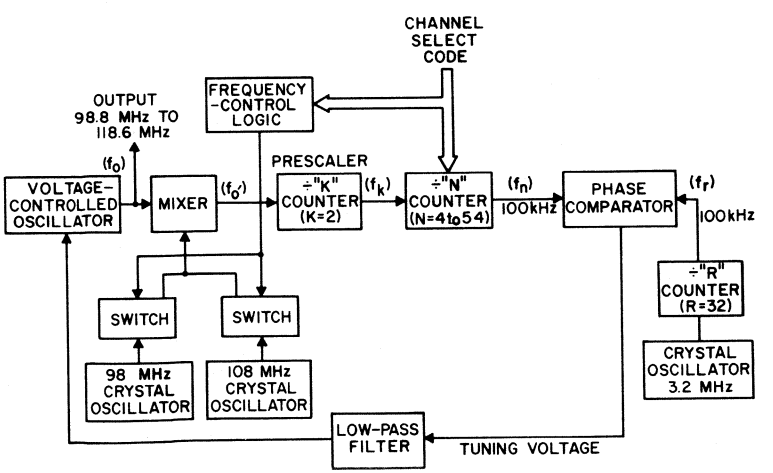


Fig.215 - Heterodyne down-conversion synthesizer.

In order to simplify the correspondence between switch settings and counter-preset states, a 1.2-MHz, or 6-count, positive offset is introduced into the divide-by-N counter design so that the range of N is actually 10 to 60, as shown in Table XXVII. For receiver frequencies between 98.1 MHz and 107.9 MHz, 108 MHz is mixed with the VCO output frequencies to down-convert to the 0.8-to-10.8 MHz range. Thus, the divide-by-N counter is "folded" and actually runs through the same count sequence for both ranges of the band, as illustrated in Table XXVII.

Fig. 215 shows that the heterodyne system requires a divide-by-2 prescaler. Thus, the phase comparison reference frequency is given by

$$f_k = \frac{200\ \text{kHz}}{2} = 100\ \text{kHz}, \qquad (29)$$

Compared to the prescaling synthesizer, a 10-to-1 improvement in loop bandwidth becomes apparent.

Because the divide-by-N counter is required to span a count range of 10 to 60, one less decade is required in the logic of the divide-by-N counter. Such a divide-by-N counter operates in a fashion similar to the one shown earlier in Fig. 199. Power consumption for this counter is approximately 40 milliwatts at the 5.4-MHz input rate for a V_{DD} of 10 volts.

Even though the divide-by-R counter consists of only five stages, instead of eight stages as needed for the prescaling system, power consumption again is concentrated in the first few flip-flops. The divide-by-R counter power dissipation is approximately 9 milliwatts at 3.2 MHz with a V_{DD} of 10 volts.

The phase comparator required by the heterodyne system of Fig. 215 operates at 100 kHz as distinguished from the frequency of 10 kHz used in the prescaling system. Power consumption is approximately 30 milliwatts for a sample-and-hold circuit design.

Table XXVII — Heterodyne Down-Conversion Operation

CHANNEL NO.	RECEIVER FREQUENCY (fm) MHz	LOCAL OSC. INJECTION FREQUENCY (f_o) (fm + 10.7 MHz) MHz	DOWN-CONVERSION FREQUENCY MHz	f_o (as in Fig. 215) MHz	N COUNT	PRESET FREQUENCY OFFSET (f_o' + 1.2 MHz) MHz	N-COUNT ACTUAL PRESET (N + 6)
1	88.1	98.8	98	0.8	4	2	10
50	97.9	108.6	98	10.8	54	12	60
51	98.1	108.8	108	0.8	4	2	10
100	107.9	118.6	108	10.8	54	12	60

As noted previously, the heterodyne system (Fig. 215) requires a prescaler of 2 operating at up to 10.8 MHz. Although a COS/MOS flip-flop can be used at this frequency, lowest power may be achieved by use of a discrete flip-flop. Power could be less than 5 milliwatts.

Power consumption for the heterodyne type of FM synthesizer is summarized in Table XXVIII. Total power consumption is shown to be approximately 146 milliwatts, 58 milliwatts less than the 204 milliwatts consumed by the prescaling system.

Preset Channel Memory

One of the many advantages of digitally tuning communications sets is the added versatility of control that emerges. For example, the digital channel-select word can be used to drive a digital display showing channel number and frequency. Another technique often employed is to control the set remotely through a hard-wired serial bit-stream of data or through transmission and reception of a digital word.

When low-voltage COS/MOS integrated circuits are used to implement digital tuning, their cost effectiveness permits adding a small preset channel memory to the system using the COS/MOS ultra-low-power memory capability. For example, a 4-word-by-9-bit memory can be used to set up, by push button or rotary switch, four favorite FM stations within a given reception area.

A suitable preset memory scheme is shown in Fig. 216. When S_1 is closed, the memory is powered from the primary system power source. However, when S_1 is opened and the set turned off, the small

Table XXVIII — Power Consumption of Heterodyne Synthesizer

FUNCTION	FREQUENCY RANGE MHz	POWER CONSUMPTION mW
DIVIDE-BY-N COUNTER	0.4 to 5.4	40
DIVIDE-BY-R COUNTER	1.6	9
CRYSTAL OSCILLATOR	1.6	2
PHASE COMPARATOR	0.1	30
DIVIDE-BY-K COUNTER	0.8 to 10.8	5
VCO (ESTIMATED)	98.8 to 118.6	25
MIXER AND OFFSET OSCILLATOR (ESTIMATED)	98 to 118.6	35
		146 Total

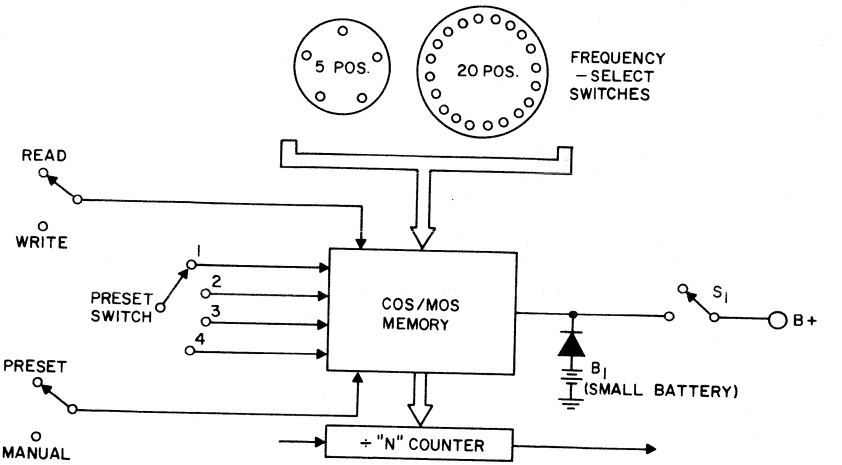


Fig.216 - Digital preset channel-memory concept.

3-volt battery supplies the few microamperes required to hold the memory in a non-volatile condition. Preset channels are written into the memory by setting up the selected channel on the frequency-select switches and switching the R/W switch to Write. The channel-select word is written into one of four words selected by the preset-switch. By setting the R/W switch to Read and the P/M switch to Preset, the N counter is thereby preset to retrieve any one of four selected words. When the P/M switch is in Manual, the frequency-select switches control the divide-by-N counter directly.

Fig. 217 illustrates mechanization of a 4-word-by-9-bit preset channel memory using two COS/MOS CD4039A scratch-pad memories. This memory chip is a 4-word-by-8-bit unit with all of the requisite control inputs, as shown in Fig. 216 and described in the paragraph above. The circuit is easily expandable in both word-length and bit-length by direct connections, needing no additional interfacing gates.

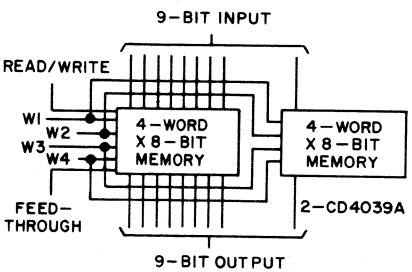


Fig.217 - Preset channel-memory circuit.

The preset channel memory using the CD4039A offers many advantages in system cost, size, and performance. For example, the preset channel memory shown in Fig. 217 costs less than $10 per chip and dissipates approximately 0.5 microwatt at a 3-volt holding potential.

Either ordinary flash-light batteries or trickle-charge batteries can be used to provide long periods of maintenance-free operation.

Linear Biasing of COS/MOS Inverters

Although COS/MOS IC's are particularly well suited for use in digital logic applications, they are also useful in many linear applications. COS/MOS inverters, when biased in the linear portion of their transfer characteristic, can be used in circuits such as linear amplifiers, threshold detectors, and oscillators. COS/MOS amplifiers offer extremely high input impedance (approximately 10^{11} ohms), low-power operation, excellent linearity, excellent temperature stability, and high gain. This section describes several methods of biasing COS/MOS devices in the linear region.

SINGLE-RESISTOR BIASING METHOD

Fig. 218 shows a COS/MOS amplifier circuit consisting of a COS/MOS inverter (1/3-CD4007A), an input capacitor for ac coupling, and a large resistor connected from input to output. The resistor biases the COS/MOS IC in the linear region of its transfer characteristic. Because the gate current is negligible, no voltage drop exists across the biasing resistor, and the amplifier is biased at the point at which $V_O = V_{IN}$, in the linear region. The range of transfer characteristics and typical curves at

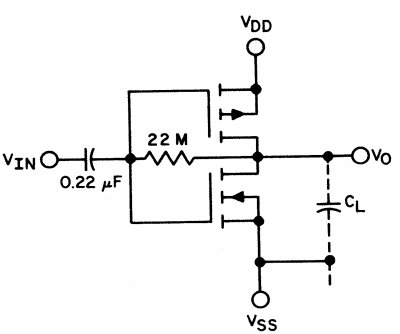


Fig. 218 - Single-stage resistor biasing method.

supply voltages of 3.5, 10, and 15 volts (V_{SS} = OV) are shown in Fig. 219. The bias points for the single-resistor biasing method occur at the intersection of a transfer curve and the line satisfying the equation $V_O = V_{IN}$.

The gain of an amplifier is equal to the slope of the transfer characteristic at the bias point; therefore, to

obtain maximum gain and linearity, the bias point for a COS/MOS amplifier should be chosen such that $V_O = V_{DD}/2$. Fig. 219 shows that for the single-resistor biasing method, the equation can be satisfied only

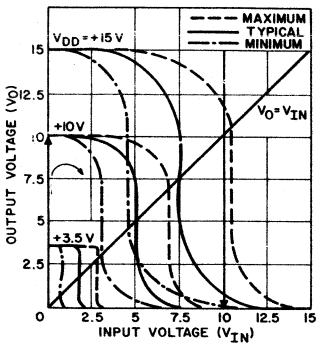


Fig. 219 - COS/MOS voltage transfer characteristics.

through the use of a COS/MOS inverter that has a transfer characteristic that satisfies the equation $V_{IN} = V_O = V_{DD}/2$. Thus, an optimum bias point cannot be established with the circuit of Fig. 218 if the inverter used does not have an ideal transfer curve unless one of the biasing methods shown in Fig. 220 is used.

TRIMMING-RESISTOR BIASING METHODS

The amplifiers in Fig. 220 are biased at $V_O = V_{DD}/2$ by trimming R1 so that the following equations are satisfied for $V_O = V_{DD}/2$. For Fig. 220(a),

$$V_{IN} = V_O \frac{R_2}{R_1 + R_2}\Bigg|_{V_O = V_{DD}/2} \qquad (30a)$$

$$= \frac{V_{DD}}{2} \frac{R_2}{R_1 + R_2}$$

For Fig. 133(b)

$$V_{IN} = V_O + \frac{(V_{DD} - V_O)R_2}{R_1 + R_2}\Bigg|_{V_O = V_{DD}/2}$$

$$= \frac{V_{DD}}{2}\left(1 + \frac{R_1}{R_1 + R_2}\right) \qquad (30b)$$

As shown in Fig. 219, the loci of Eq. (30a) are lines which pass through the origin and whose slope is dependent on the value of R1 (R2 is a constant; therefore the slope is greater than or equal to 1). The loci of Eq. (30b) are lines which pass through the point V_O = 10 volts, V_{IN} = 10 volts (V_{DD} = 10 volts) and whose slope (less than or equal to 1) is also dependent

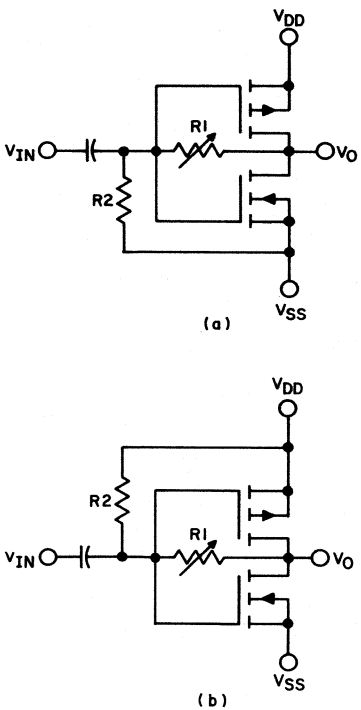


Fig. 220 - Trimming-resistor biasing methods.

on R1. The bias point is the intersection of the transfer characteristic at $V_O = V_{DD}/2$ and the line obtained from either Eq. (30) or Eq. (31) for given values of R1 and R2. The entire transfer plane is covered by the three biasing methods mentioned [Figs. 218, 220(a), 220(b).] Thus, biasing at $V_O = V_{DD}/2$ can always be accomplished by custom selection of bias resistor R2 (Fig. 220) for each amplifier.

The biasing methods shown in Fig. 220 are especially useful in digital shaping applications in which the amplifier is designed to clip. The bias point can be adjusted to one side of $V_O = V_{DD}/2$ for any desired noise immunity; i.e., threshold-detection application. In linear applications, the single-resistor biasing method is usually adequate; the lower gain achieved through the use of the minimum and maximum transfer curves is usually acceptable. If the lower gain is not acceptable, however, and adjustment of R1 is undesirable, additional stages could be cascaded after the first biased stage to provide additional amplification.

PERFORMANCE

Performance of the biasing circuits in Figs. 218 and 220 is not dependent on one biasing voltage, but is dependent on the transfer characteristic of the amplifier. Excellent bias-point stability is, therefore, possible. The transfer characteristics shift slightly ($\Delta V_{IN} \approx 0.3$ volt) over a -55°C to +125°C temperature range, but the biasing methods shown maintain the bias point in the linear region despite temperature variations.

As shown in Fig. 219, COS/MOS IC's have extremely sharp transfer characteristics in the linear region. The steepest slope occurs when $V_{DD} = V_{TH(n)} + V_{TH(p)}$, where $V_{TH(n)}$ and $V_{TH(p)}$ are the n- and p-channel theshold voltages, respectively. With this condition satisfied, the transfer characteristic is approximately a vertical line. COS/MOS amplifiers, then, have the greatest gain when $V_{DD} = V_{TH(n)} + V_{TH(p)}$. The transition region is also linear over the greatest percentage of the supply voltage under this condition. As V_{DD} increases above the voltage range $V_{TH(n)} + V_{TH(p)}$, the transfer region remains linear, but the slope of the linear region decreases, resulting in decreased gain.

The linear biasing concepts described in this section demonstrate the versatility of the COS/MOS technology. Applications to custom and standard products are limited only by the ingenuity of the designer.

Crystal Oscillators

Quartz-crystal oscillators have long been popular because of their excellent frequency stability and the wide range of frequencies over which they can be used. COS/MOS crystal-oscillator circuits provide the additional advantages of low power consumption and stable operation over a wide range of supply voltages.

This section describes the design of COS/MOS crystal-controlled oscillators. The CD4007A COS/MOS inverter is used in the design examples.

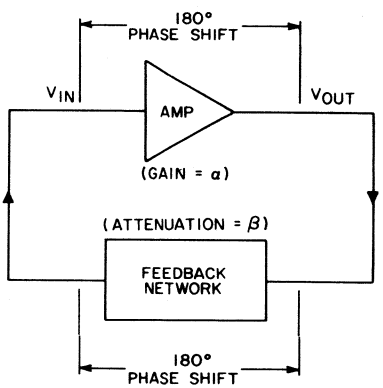


Fig. 221 - Basic crystal-oscillator circuit.

BASIC CIRCUIT

The design of a COS/MOS crystal-oscillator circuit, as the design of any crystal-oscillator circuit, involves the design of a feedback and an amplifying section. The basic circuit configuration is shown in Fig. 221.

To determine the conditions for oscillation, a small falling input (V_{IN1}) may be supplied to an amplifier with an inherent 180° phase shift between its input and output. The output of the amplifier (V_{O1}) is then a rising waveform of amplitude αV_{IN1}. If this signal is then applied to a feedback circuit which itself causes an additional 180° phase shift, the amplifier input (V_{IN2}) is an attenuated rising signal of amplitude βV_{O1} whose phase lags V_{O1} by 180°. This rising signal causes an amplified falling signal (V_{O2}) of magnitude αV_{IN2} to appear at the amplifier output. If V_{O2} is less than or equal to V_{O1}, this cycle continues and sustains oscillation. However, V_{IN2} is equal to βV_{O1} and V_{O2} is equal to αV_{IN2};

therefore, V_{O2} is equal to $a\beta V_{O1}$. Because oscillation requires that V_{O2} be less than or equal to V_{O1}, one of the conditions for oscillation is that $a\beta$ be less than or equal to 1. For oscillation to begin, however, $a\beta$ must be greater than and not equal to 1; thus, oscillators must be designed to satisfy this criterion. The other criterion for oscillation, as noted above, is that the phase shift around the loop be $n360^o$.

CRYSTAL CHARACTERISTICS

An understanding of crystal-oscillator circuits requires an understanding of the crystal itself or, more specifically, the equivalent electrical circuit of a quartz crystal, as shown in Fig. 222. Typical values of the parameters used in Fig. 135 are given in Table XXIX.

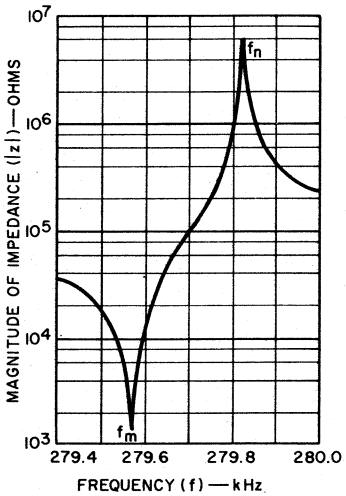


Fig. 223 - Magnitude of the impedance of a crystal as a function of frequency.

The crystal parameter values used are those of a crystal having a series

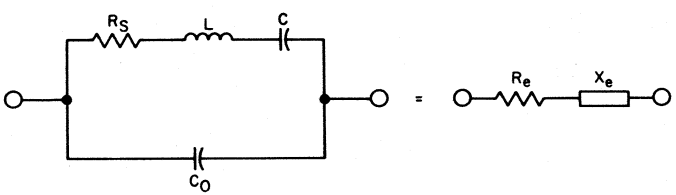


Fig.222 - Equivalent electrical circuit of a quartz crystal.

Table XXXI – Typical Crystal Parameter Values

Parameter	Frequency			
	90 kHz	280 kHz	525 kHz	2 MHz
R_S (ohms)	15 k	1.35 k	220	150
L (H)	137	27.7	7.8	0.785
C (pF)	0.0235	0.0117	0.0115	0.00135
Co (pF)	3.5	6.18	6.3	3.95

Fig. 223 shows a graph of the magnitude of the impedance of a crystal as a function of frequency. resonant frequency (f_S) of 279.569 kHz (280-kHz column in Table XXIX). Figs. 224 through 226 show graphs of the impedance angle (ϕ_c) as a function of frequency and the equivalent resistive (R_e) and reactive (X_e) components of the impedance. The reactance curve (X_e) of Fig. 224 shows that the crystal appears purely resistive at two points where $X_e = 0$. These two points are defined at the resonance (f_r) and antiresonance (f_a) frequencies. Fig. 224 shows f_r to be

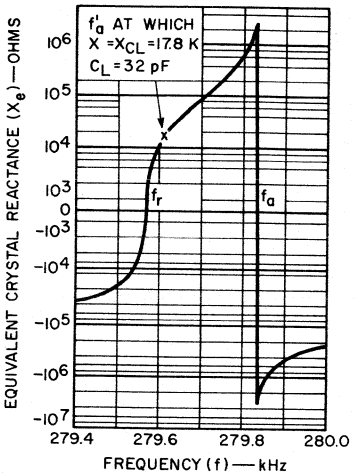


Fig.224 - Equivalent crystal reactance as a function of frequency.

approximately 279.569 kHz, equal, at first glance, to the frequency of minimum impedance f_m (Fig. 223) and to the series-resonant frequency. This equality would indeed be true with $R_S = 0$. Actually, f_m is less than f_s which is less than f_r, but these frequencies may be considered equal for this discussion because, for typical values of R_S, the difference between them is within a few parts per million. Similarly f_a, f_p, and f_n may be considered equal. Fig. 223 shows that only a small frequency difference exists between the maximum and minimum impedance points.

It may be shown that

$$f_a \approx f_s\left(1 + \frac{C}{C_O}\right)^{1/2} \qquad (31)$$

The ratio C/C_O is typically about 0.003. Then f_a is approximately equal to 1.0015 f_s. Virtually all crystal oscillators are designed to operate between f_s and f_a; therefore the frequency difference is important.

Values of R_e and X_e are important considerations when designing for maximum oscillator stability. At the resonance and antiresonance frequencies, $X_e = 0$. The magnitude of the crystal impedance Z becomes

$$|Z| = \sqrt{R_e^2 + X_e^2}$$
$$= R_e \qquad (32a)$$

The impedance at $f_s \approx f_r$ is equal to the impedance of R_S in parallel with C_O. Because X_{CO} is much greater than R_S in a good crystal, $|Z| \approx R_S$; therefore, at series resonance, $R_e \approx R_S$ is shown by Figs. 223 and 225.

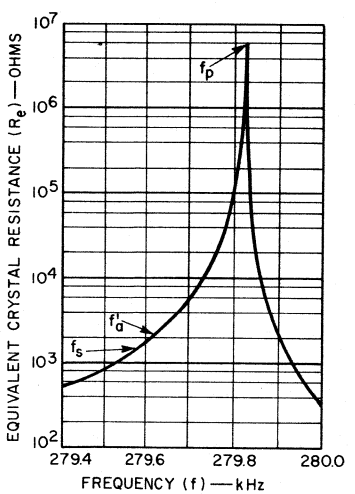


Fig.225 - Equivalent crystal resistance as a function of frequency.

FEEDBACK NETWORK

Another important consideration in a stable oscillator design is the rate of change of feedback-network phase

angle, ϕ, with frequency. One of the conditions for oscillation is that the phase angle around the loop be equal to n360°. If the amplifier phase shift is 180°, the feedback network must provide an additional 180° of phase shift. Because of inherent propagation delays, however, the amplifier phase shift is not precisely 180°. Furthermore, the propagation delay in the amplifier is variable as a result of supply-voltage variations and/or variations in semiconductor performance with temperature changes. To maintain a 360° loop phase shift, the feedback network must provide a phase change to compensate for any change in amplifier phase shift. The result is a frequency shift, which, as in the case of a stable oscillator, is small if $d\phi/df$ is maximized.

The rate of change of feedback-network phase angle with frequency is directly related to the phase-changing properties of the crystal. Fig. 226 shows that a high rate of change of impedance angle with frequency occurs at the resonance and antiresonance frequencies. The high $d\phi/df$ is a result of the high $Q = \omega_0 L/R_S$ of the equivalent circuit. Maximum $d\phi/df$ occurs with maximum Q or when R_S is a minimum. With $R_S = 0$, Fig. 226 appears as two vertical lines at f_r and f_a, indicating infinite $d\phi/df$. For maximum frequency stability, then, it is desirable that R_S be minimum.

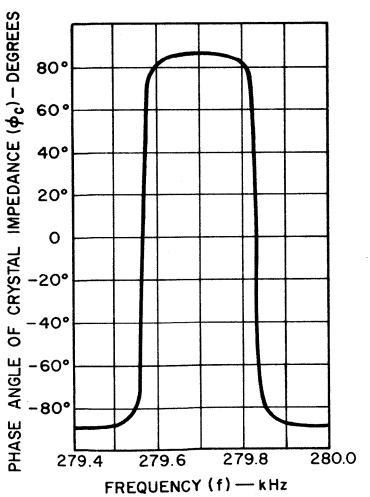


Fig.226 - Phase-angle of crystal impedance as a function of frequency.

Fig. 223 shows that the impedance of the crystal increases rapidly as f_a is approached. For this reason, most crystal-oscillator circuits are designed to operate or at near series resonance. Operation at antiresonance is impractical, not only because of the extremely high input impedance, but also because of the frequency dependence on C_O. Stray capacitance in the circuit layout is usually significant when compared with C_O; therefore, wide variations in frequency can occur with various circuit layouts. The frequency becomes less dependent on C_O as f_s, is approached and is completely independent of C_O at f_s.

RESONANCE AND ANTIRESONANCE

A method of reducing the frequency dependence on C_O is to manufacture the crystal to resonate at the design frequency with a specified value of external loading capacitance. A load capacitor C_L could be placed in parallel with the crystal, thereby effectively increasing C_O and greatly reducing the effect of circuit stray capacitance if C_L is sufficiently large. The presence of C_L also decreases the impedance viewed

across the crystal terminals. Both considerations make operation at antiresonance more practical.

Another method of operation is to place the loading capacitor in series with the crystal. The effective resistance R_e of the series circuit will not change; however, the reactance becomes $X_e - X_{CL}$. The frequency of minimum impedance will again occur when the total reactance is zero or when $X_e = X_{CL}$. Fig. 224 shows a frequency f'_a of about 279.611 kHz at which $X_e = X_{CL} =$ 17.8 kilohms of $C_L = 32$ picofarads. Because $X_e - X_{CL} = 0$ at this frequency, the magnitude of crystal impedance Z becomes

$$Z = \sqrt{R_e^2 + (X_e - X_{CL})^2}$$
$$= R_e \qquad (32b)$$

To keep R_e small, then, f'_a should be close to f_s. C_L, however, becomes infinite as f_s is approached. Therefore, f'_a should not be chosen so close to f_s that the large values of C_L required cannot satisfy the gain and phase requirements of the oscillator circuit. Values of C_L of 20 and 32 picofarads are usually used.

The frequency f'_a at which $X_e = X_{CL}$ is approximately equal to the antiresonance frequency of the crystal with the same value of C_L as a parallel loading capacitor. The crystal impedance at f'_a however, differs for the two cases. With a series loading capacitor it has been shown that $|Z| = R_e \approx 1.9$ kilohms at f'_a, as shown in Fig. 225. The impedance (with a parallel loading capacitor of 32 picofarads) can be calculated. With $C_O = 32 + 6.18 =$ 38.18 picofarads, $|Z|$ is 155 kilohms at f'_a or many times greater than 1.9 kilohms. The $d\phi/df$ is also greater for a series loading capacitor than for a capacitor in parallel with the crystal. Therefore, a series loading capacitor is generally preferred.

Crystals manufactured to resonate at the stamped design frequency, then, will oscillate with a parallel loading capacitor at the antiresonant frequency f'_a of the combination and with a series loading capacitor at the series-resonant frequency (again f'_a of the combination). Such crystals are called antiresonant crystals and are used in antiresonant oscillator circuits as distinguished from series-resonant crystals designed to oscillate at f_s in series-resonant oscillator circuits. The term "antiresonant oscillator circuit" is perhaps a misnomer. When operating with a series loading capacitor the circuit oscillates somewhere between f_s and f_a and not at the true antiresonant frequency of the crystal.

Both types of oscillator circuits employ the general circuit configuration shown in Fig. 221. However, the design of the amplifying and feedback sections differs. Antiresonant oscillator circuits with a series loading capacitor are most applicable to COS/MOS crystal-oscillator circuits and are the types discussed subsequently.

COS/MOS OSCILLATOR CIRCUITS

A good amplifier for the amplifying section of the oscillator is a COS/MOS inverter with a large resistor connected from the input of the inverter to the output as shown in

Fig. 227. The value of R_f should be large enough (greater than or equal to 10 megohms) that the attenuation and phase of the feedback network are not appreciably affected. The

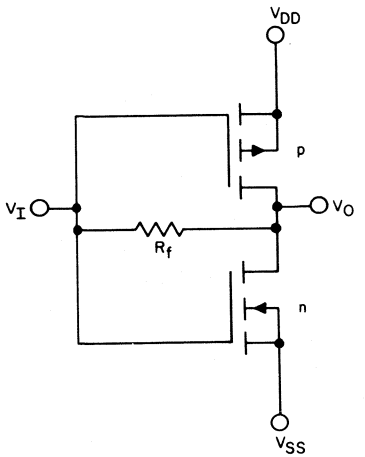


Fig.227 - Typical COS/MOS inverter with feedback resistor.

resistor dc biases the output voltage at the point at which $V_O = V_{IN}$. This point is typically at or near one-half of the supply voltage, as noted from the typical COS/MOS-inverter transfer characteristics shown in Fig. 228.

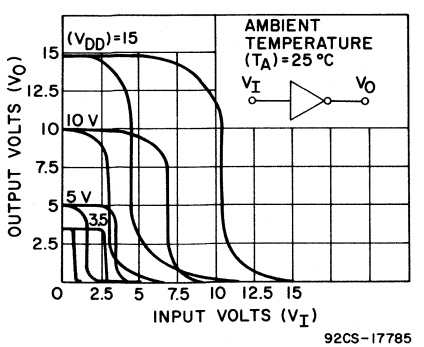


Fig.228 - Typical COS/MOS inverter transfer characteristics.

With V_{DD} = 10 volts, a ±1-volt swing around the bias point causes an output swing of approximately 10 volts; thus, the voltage gain (K_A) of the amplifier for a full swing is about 5. The transfer characteristics become sharper as the supply voltage is reduced, and the gain at a V_{DD} of 5 volts increases to about 10. An oscillator circuit, then, may be formed using the amplifier described with a feedback network having an attenuation constant (β) greater than 0.2.

The feedback circuit should not only be capable of β greater than 0.2, but should also maintain a high rate of change of phase angle with frequency ($d\phi/df$) and be designed so that the interchanging of any oscillator component does not cause a significant shift in the frequency of oscillation. Fig. 229 shows a crystal pi-network circuit which will accomplish these objectives with the correct choice of component values.

A COS/MOS crystal-oscillator circuit may be designed for any crystal provided the value of its maximum equivalent resistance at a specified value of loading capacitance C_L is known. A crystal which resonates in antiresonant oscillator circuits at 279.611 kHz with C_L = 32 picofarads will serve as a design example. The characteristics of this crystal were presented in Figs. 223 through 226; an equivalent resistance of 1.9 kilohms was found at f'_a = 279.611 kHz. If this value is used for R_e, however, the results obtained would apply only to this particular crystal. Equivalent resistances of crystals manufactured to resonate at the same frequency can vary by an order of magnitude. The important

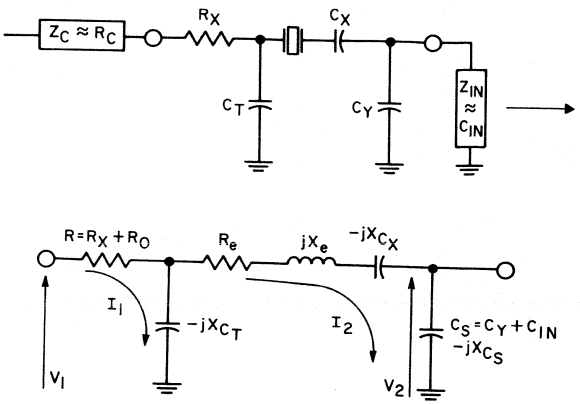


Fig.229 - Crystal pi network.

value of R_e is the maximum value of equivalent resistance.

Design Equations

The design begins with a calculation of the voltage gain K_A, as follows:

$$K_A = \frac{4(X_e - XC_X) + 1.07\ R_e}{X_e - X_{C_X} - 1.07\ R_e\beta} \qquad (33)$$

In COS/MOS oscillator circuits, C_X can usually be eliminated; then XC_X is zero in Eq. (33). It may, however, be desirable to include C_X in some cases to allow an increase in the value of C_S and a decrease in the frequency dependence on the input capacitance of the COS/MOS inverter. With XC_X = 0, however, the values of C_S obtained are usually much larger than the individual variations in inverter input capacitance.

The value of R_{emax} to be used in Eq. (33) is usually supplied by the crystal manufacturer and is specified as 2.5 kilohms for the 279.611-kHz crystal used in this example. X_e = XC_L for C_L = 32 picofarads, and was found previously to be 17.8 kilohms. With R_e = 2.5 kilohms, X_{CX} = 0, and β = 0.75, K_A is calculated as 4.67. This value is substituted in the following equation:

$$X_{L\,(eff)} = \frac{X_e - X_{C_X}}{1 + \beta K_A} \qquad (34)$$

$X_{L(eff)}$ is then determined to be 3.96 kilohms. X_{C_T} is equal to $X_{L(eff)}$, and is thus also equal to 3.96 kilohms. XC_S is given by

$$XC_S = \beta\, X_{L(eff)}\, K_A \qquad (35)$$
$$= 13.9 \text{ Kilohms}$$

The value of R is determined as follows:

$$R = (K_A - 1)\left(\frac{X_{L(eff)}{}^2}{R_e}\right)$$
$$= 23 \text{ Kilohms} \qquad (36)$$

Values of C_S and C_T are calculated from the following relation:

$$C_{(S,T)} = \frac{X_e C_L}{X_{C(S,T)}} \qquad (37)$$

With C_S = 41 picofarads and C_T = 142 picofarads, a check should be made to assure that $1/C_L = 1/C_T + 1/C_S$; in this case, $1/31 \approx 1/41 + 1/142$. The circuit, then, should oscillate at or near 279.611 kHz with R = 23 kilohms, C_S = 41 picofarads, and C_T = 142 picofarads provided the amplifier phase lag is equal to or near the phase lead of the feedback circuit at f'_a.

Because the output impedance of a COS/MOS inverter is typically 1 kilohm, a value of 22 kilohms should be used for R_X (Fig. 229). To obtain the value of C_y, the value of C_S should be reduced by the value of the wiring and input capacitance, including the increase in C_{IN} due to the Miller effect, as follows:

$$C_y = C_S - 10pF \qquad (38a)$$

when $1.5\,V \leq V_{DD} \leq 5V$, and

$$C_y = C_S - 15pF \qquad (38b)$$

when $5\,V \leq V_{DD} \leq 15\,V$.

In addition, a small trimmer capacitor for trimming to the design frequency should be added in parallel with C_T. The trimmer capacitor should have a maximum value of about 30 per cent of the calculated value of C_T, and the actual value of C_T should be chosen so that C_T plus the mid-range value of the trimmer capacitor equals the calculated value of C_T. The complete COS/MOS crystal-oscillator circuit incorporating the 279.611-kHz crystal is shown in Fig. 230. Standard component values close to those calculated are used.

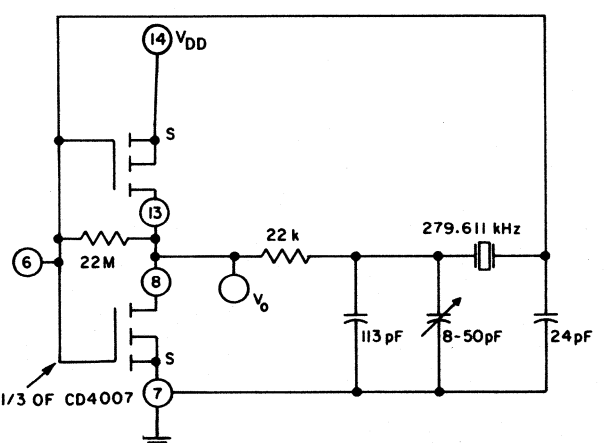


Fig.230 - CD4007A COS/MOS crystal-oscillator circuit incorporating the 279.611-kHz crystal.

Performance

Figs. 231 and 232 show calculated results for the phase shift versus frequency and for β versus frequency

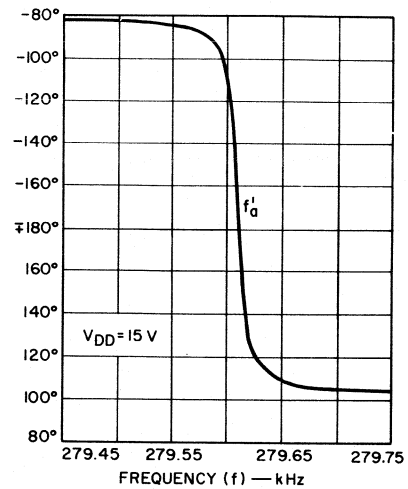


Fig. 231 - Feedback-network phase angle as a function of frequency for the circuit of Fig. 230.

for the 279.611-kHz oscillator. The figures show that $d\phi/df$ and β are greatest at 279.611 kHz or when $X_e = X_{CL}$. From Fig. 231, the frequency is seen to change by about 1.2 cycles for $\Delta\phi = 15^o$. The stability of the oscillator may then be predicted at 1.2/279.611 = 4.3 parts per million assuming only a phase change in the amplifier. The actual stability, of course, is somewhat less because of variations in crystal parameters and component values with temperature changes.

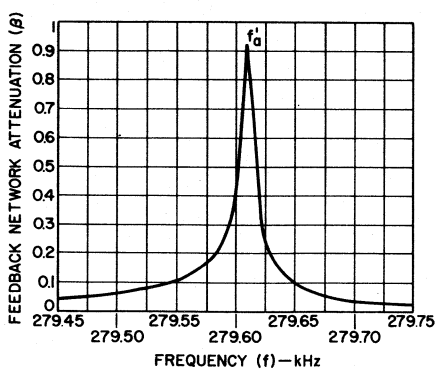


Fig.232 - Feedback-network attenuation as a function of frequency for the circuit of Fig. 230.

The values of components in Fig. 230 apply only when the 279.611-kHz crystal is used. Values of C_S and C_T remain close to 41 picofarads and 142 picofarads if C_L = 32 picofarads, and K_A is chosen from Eq. (33) with β = 0.75 and XC_X = 0. The value of R, however, will change according to the maximum equivalent resistance of the crystal used. The number of different component values satisfying the design equations for different oscillator specifications is virtually infinite; the component values given in Fig. 230 represent only a typical case. The design equations have been derived to allow freedom of design for desired characteristics.

Supply-Voltage Considerations

The COS/MOS crystal-oscillator circuit shown in Fig. 230 may be operated at supply voltages from 5 to 15 volts. For lower current drain, the circuit may be modified as shown in Fig. 233 by adding resistors in the supply and ground lines when a full V_{SS}-to-V_{DD} output-voltage swing is not required. The value of R_X in this circuit should be reduced by the amount of the added resistance.

Experimental data on the oscillator circuits shown in Figs. 230 and 231 are given in Tables XXX and XXXI.

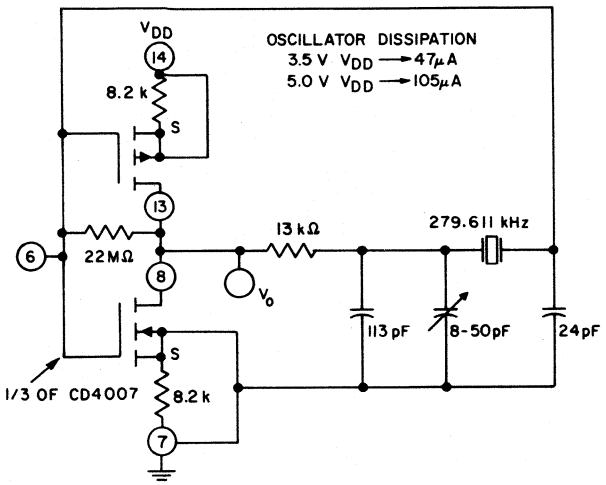


Fig.233 - Crystal-oscillator circuit using the CD40027A; V_{DD} less than 15 volts.

Table XXX – Conditions Causing Change of Frequency in Circuits of Fig. 230

Condition	Frequency Change (Parts/Million)
-40° to +85° change in ambient temperature:	
on COS/MOS unit alone	4
on the complete oscillator (mica capacitors, carbon resistors)	55
+25% change in V_{DD} T_A = 25°C	+3.5
-25% change in V_{DD} T_A = 25°C	-3.5

Table XXXI – Supply Voltage and Average Supply Current for COS/MOS Crystal Oscillators

Supply Voltage (Volts)	Average Supply Current (Microamperes)	Circuit
2.5	23	Fig. 230
3.5	47	↓
5.0	105	↓
6.0	86	Fig. 233
10.0	200	↓

Operating Frequencies

A wide range of frequencies is attainable with COS/MOS crystal-oscillator circuits. Frequencies up to about 10 MHz are possible at a V_{DD} of 15 volts. Beyond 10 MHz, $\Delta\phi$ becomes too large, and stability decreases accordingly. The lowest frequency of operation depends only on the equivalent resistance of the crystal. Values of R_S and R_e increase rapidly at the lower frequencies and require amplifiers with high input impedance to minimize the attenuation (β) across the feedback network. Because COS/MOS amplifiers have high input impedances of approximately 10^{11} ohms, much lower frequencies are possible in COS/MOS antiresonant-oscillator circuits than in bipolar-transistor antiresonant circuits. Frequencies down to 2 kHz

have been achieved with three inverters (one CD4007A) connected in parallel to provide the greater current drive required by the crystal at this frequency.

Frequencies lower than 2 kHz are easily obtained by counting down the oscillator frequency. For example, a 16.384-kHz oscillator could be used with a 14-stage binary counter with the fourteenth stage counting at one pulse per second. A functional diagram for this type of circuit is shown in Fig. 234.

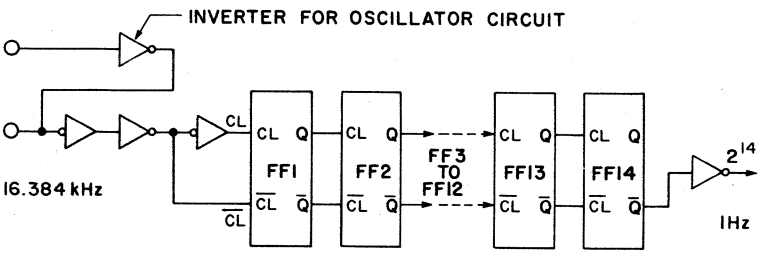


Fig. 234 - Functional diagram of a COS/MOS oscillator interconnected with a 14-stage binary counter.

Circuits

This section illustrates a variety of circuit ideas that can be readily implemented by use of the RCA-CD4000A series of COS/MOS integrated circuits. Logic functional diagrams and operating waveforms are shown for a broad range of circuits in which the low quiescent dissipation, well-defined logic levels, high noise immunity, and other features of the CD4000A-series devices result in significant advantages. Brief summations are given of the over-all logic function of the various circuits. Detailed information on the operation of basic circuit elements, such as gates, inverters, flip-flops, counters, and registers, that may be included in the various circuit arrangements are given in earlier sections of this Manual.

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19	Four-Channel Time-Division Multiplexer	217
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21	Digital Ramp Generator	218
22	Party-Bit Generator	219
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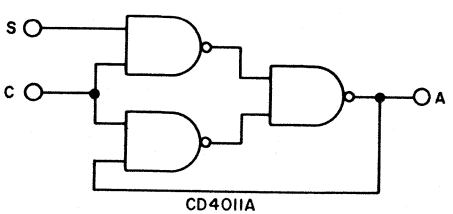
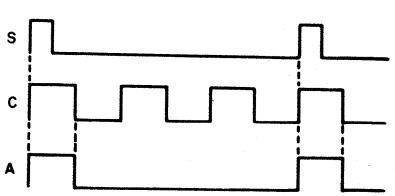
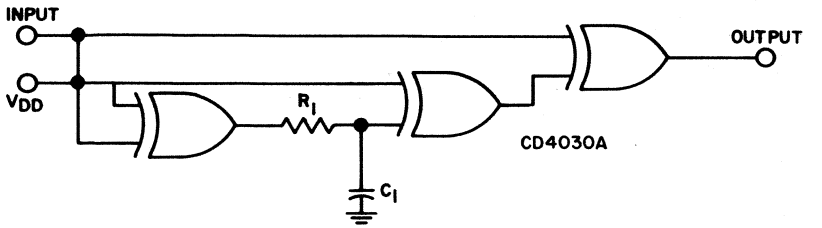
CIRCUIT NO. 1 – PULSE STRETCHER

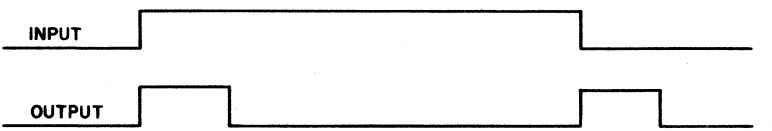
This circuit illustrates the use of the CD4011A Quad 2-input NAND gate as a pulse stretcher. The signals at terminals S and C are synchronized. The pulse duration of the signal at terminal S, however, is much shorter that that of the signal at terminal C. The feedback loop from the output (terminal A) stretches out the pulse at S to equal the length of the pulse at C. Any time the pulse at S is not present, the output is zero. The repetition rate of C can, therefore, be any convenient multiple of the basic S rate. The output signal has a pulse duration equal to that of the signal applied to terminal C and the same repetition rate as the signal applied to terminal S. The circuit waveforms shown indicate the relationship between output and input pulses when the repetition rate of the signal at C is three times that of the signal at S.





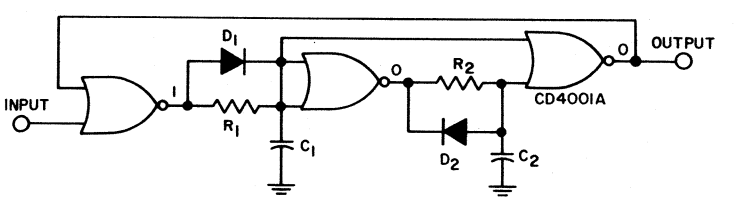
CIRCUIT NO. 2 – TRANSITION DETECTOR/FREQUENCY DOUBLER

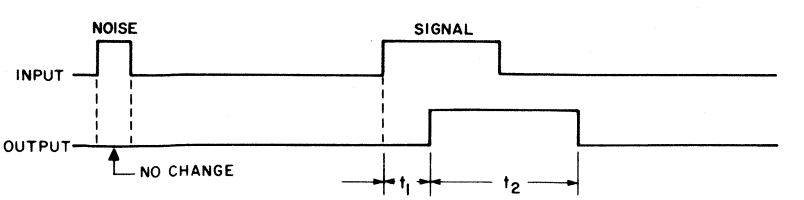




This circuit shows an arrangement for use of the CD4030A quad exclusive-OR gate to detect logic-level changes. A transition from low to high or from high to low produces a pulse at the output terminal of the CD4030A. The duration of the output pulse can be varied by a change in the time constant of the resistance-capacitance network formed by R_1 and C_1. The section of this Manual on **Astable and Monostable Multivibrators** explains how the desired values of resistor R_1 and capacitor C_1 are determined. Because two output pulses are produced for each input pulse, this circuit is also useful as a frequency doubler.

CIRCUIT NO. 3 – NOISE DISCRIMINATOR

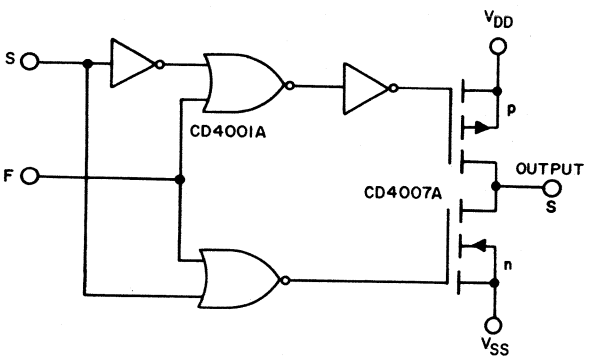




CIRCUIT NO. 3 – NOISE DISCRIMINATOR (cont'd)

In this circuit, the CD4001A quad two-input NOR gate is used in a noise-discriminator application. The circuit discriminates between noise pulses that last less than a specific duration t_1 and pulses that have a duration greater than t_1. An input pulse that has a duration greater than t_1 produces an output of pulse duration t_2. The time t_1 is determined by the time constant of resistor R_1 and capacitor C_1 (i.e., $t_1 = R_1C_1$). The time t_2 is determined by the time constant of resistor R_2 and capacitor C_2 (i.e., $t_2 = R_2C_2$). Diodes D_1 and D_2 allow fast recovery.

CIRCUIT NO. 4 – THREE-STATE BUFFER

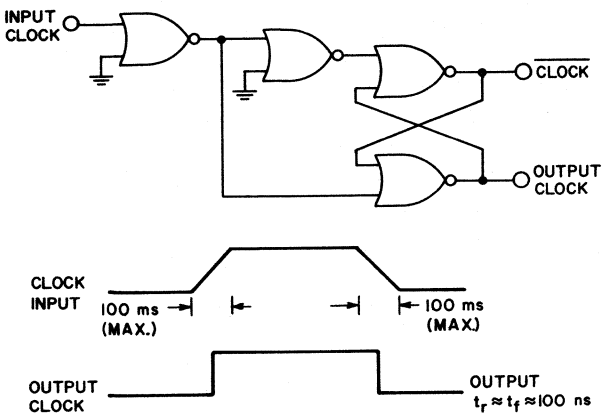


This circuit shows a three-state buffer with high source- and sink-current capability that can be constructed by use of a CD4007A dual-complementary-pair-plus-inverter circuit and a CD4001A quad two-input NOR gate plus inverter. When the input at F is low, the output has two binary states equivalent to the input at S. When the F input is high, the output is in an open circuit (both n- and p-channel devices are off) with respect to both V_{SS} and V_{DD}. This buffer can be used to connect several COS/MOS signal sources to the same line or data bus.

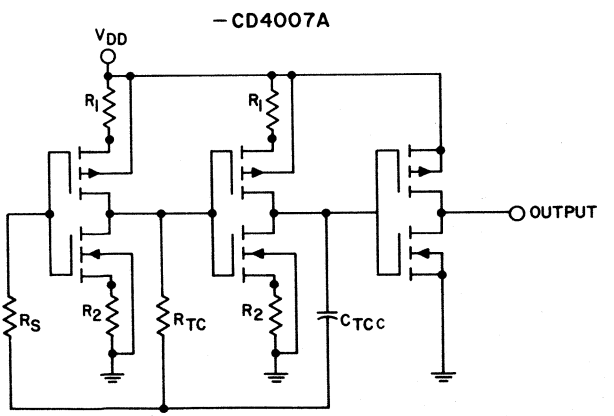
CIRCUIT NO. 5 – CLOCK-EDGE SHAPING CIRCUIT

This circuit illustrates how a CD4001A quad two-input NOR gate may be used to reshape the rise and fall times of clock pulses that have slow transition times. Shorter transition times of the output clock pulse result from the regeneration action of the output flip-flop. Complementary clock outputs are also available. With this circuit, an input clock pulse that has rise and fall times of 100 milliseconds can be reshaped so that the transition times are reduced to 100 nanoseconds.

CIRCUIT NO. 5 – CLOCK-EDGE SHAPING CIRCUIT (cont'd)



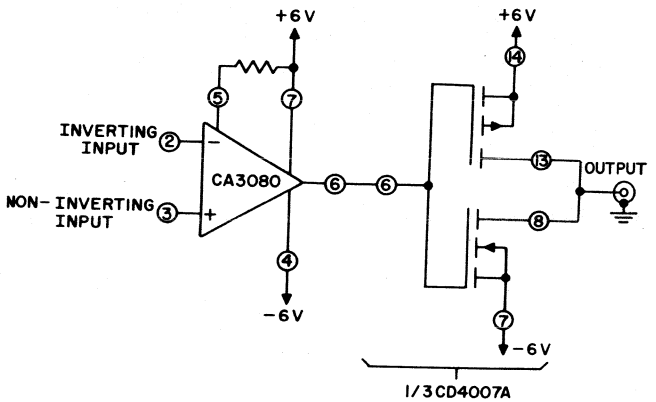
CIRCUIT NO. 6 – LOW-POWER, LOW-FREQUENCY OSCILLATOR



SEE ICAN 6267 FOR CHOICE OF R_S, R_{TC}, C_{TC}. VALUE OF R DEPENDENT ON FREQUENCY AND RISE TIME REQUIRED.

One CD4007A dual complementary pair plus inverter circuit can be wired as shown in this diagram to form a low-power low-frequency oscillator (astable multivibrator). The current-limiting resistors R_1 and R_2 result in low-power oscillation. The frequency of operation is determined by the values of resistors R_S and R_{TC} and capacitor C_{TC}. These values are selected as explained in the section on **Astable and Monostable Multivibrators.**

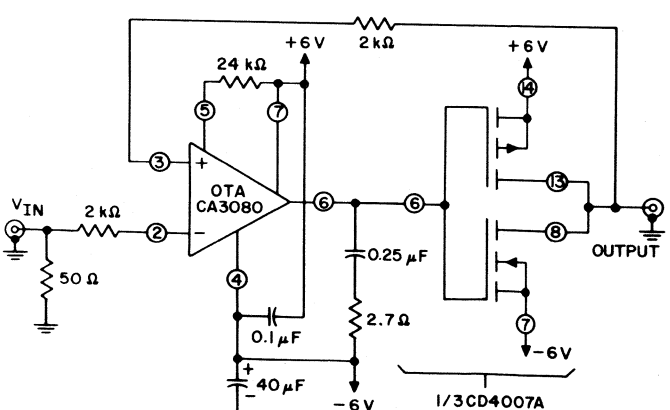
CIRCUIT NO. 7 – INVERTER/AMPLIFIER DRIVEN BY OTA (OPEN-LOOP MODE)



This circuit shows an RCA-CA3080 operational transconductance amplifier (OTA)* driving one inverter/amplifier section of the CD4007A dual-complementary-pair-plus-inverter circuit in the open-loop mode. For greater current output, the two remaining amplifiers of the CD4007A may be connected in parallel with the single stage shown. The open-loop gain of the over-all circuit is approximately 130 dB.

*Detailed descriptive information on the CA3080 is given in the RCA Technical Bulletin File No. 475.

CIRCUIT NO. 8 – INVERTER/AMPLIFIER DRIVEN BY OTA (CLOSED-LOOP MODE)



CIRCUIT NO. 8 – INVERTER/AMPLIFIER DRIVEN BY OTA (CLOSED-LOOP MODE) (cont'd)

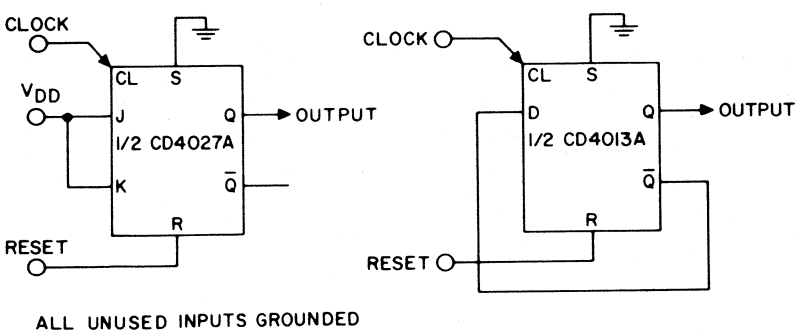
In this circuit, an inverter/amplifier section of the CD4007A dual-complementary-pair-plus-inverter circuit is driven by an RCA-CA3080 operational transconductance amplifier (OTA)* in the unity-gain closed-loop mode. For greater current output, the two remaining amplifiers of the CD4007A may be connected in parallel with the single stage shown.

*Detailed descriptive information on the CA3080 is given in the RCA Technical Bulletin File No. 475.

SEQUENTIAL COUNTERS

Sequential counters are found in almost all equipment containing digital logic. They can perform state control, timing-pulse sequencing, frequency conversion, and numerous other functions. Some appplications require counter designs which cycle through N states (a module N or divide-by-N counter). Circuits Nos. 9 through 15 show how various divide-by-N counters (ripple or synchronous) can be implemented by use of COS/MOS integrated circuits. Detailed explanations of the operation of both synchronous and ripple counters are given in the section on **Counters and Registers.**

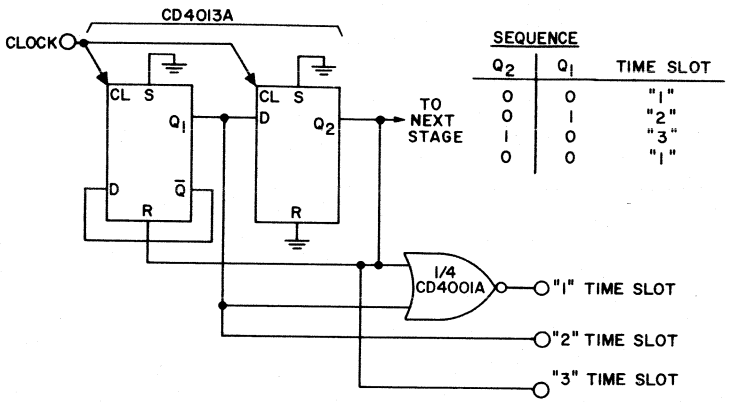
CIRCUIT NO. 9 – DIVIDE-BY-2 COUNTERS



ALL UNUSED INPUTS GROUNDED

These circuits illustrate the use of one-half a CD4027A dual J-K master-slave flip-flop and one-half a CD4013A dual "D" type flip-flop to form two simple divide-by-2 counters. The CD4013A counter is made to toggle by returning the Q output to the D input.

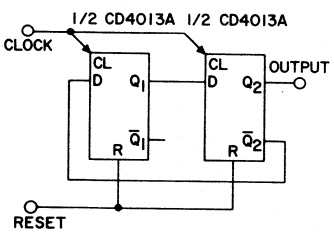
CIRCUIT NO. 10 – DIVIDE-BY-3 SYNCHRONOUS COUNTER WITH DECODED OUTPUTS



SEQUENCE		
Q_2	Q_1	TIME SLOT
0	0	"1"
0	1	"2"
1	0	"3"
0	0	"1"

In this circuit, both sections of a CD4027A dual "D" type flip-flop are interconnected with one gate unit of a CD4001 quad two-input NOR gate to form a divide-by-3 synchronous counter with three decoded outputs.

CIRCUIT NO. 11 – DIVIDE-BY-4 SYNCHRONOUS COUNTER



SEQUENCE (JOHNSON)		
Q_2	Q_1	STATE
0	0	0
0	1	1
1	1	2
1	0	3
0	0	0

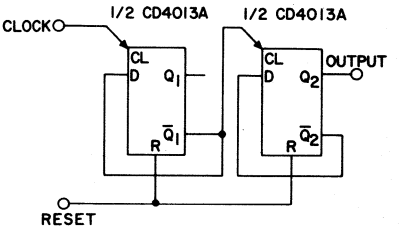
ALL UNUSED SETS GROUNDED

This circuit illustrates the use of both sections of a CD4013A dual "D" type flip-flop in a divide-by-4 synchronous counter. A high level on the reset line forces the counter into the "0" state.

CIRCUIT NO. 12 – DIVIDE-BY-4 RIPPLE COUNTER

In this circuit, the two sections of a CD4013A dual "D" type flip-flop are interconnected to form a divide-by-4 ripple counter. A comparison of the truth table for this circuit with that for Circuit No. 11 shows the variation in the logic sequences for ripple and synchronous counters that provide the same count division. As with the synchronous type shown in Circuit No. 11, a high level on the reset line forces the divide-by-4 ripple counter into the "0" state.

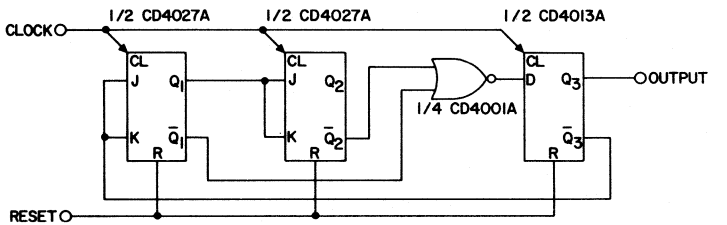
CIRCUIT NO. 12 – DIVIDE-BY-4 RIPPLE COUNTER (cont'd)



SEQUENCE

Q_2	Q_1	STATE
0	0	0
0	1	1
1	0	2
1	1	3
0	0	0

CIRCUIT NO. 13 – DIVIDE-BY-5 SYNCHRONOUS COUNTER



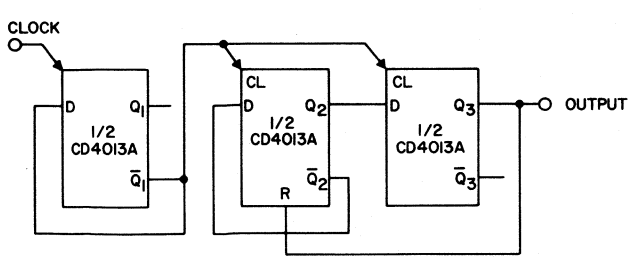
ALL UNUSED SETS GROUNDED
ALL UNUSED GATE INPUTS GROUNDED

SEQUENCE

Q_3	Q_2	Q_1	STATE
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
0	0	0	0

In this circuit, both sections of a CD4027A dual J-K flip-flop, a single gate unit of the CD4001A quad two-input NOR gate, and one section of a CD4013A dual "D" type flip-flop are interconnected to form a divide-by-5 synchronous counter. As with Circuits Nos. 11 and 12, a high level on the reset line forces the counter into the "0" state.

CIRCUIT NO. 14 – DIVIDE-BY-6 RIPPLE COUNTER



ALL UNUSED SETS AND RESETS GROUNDED

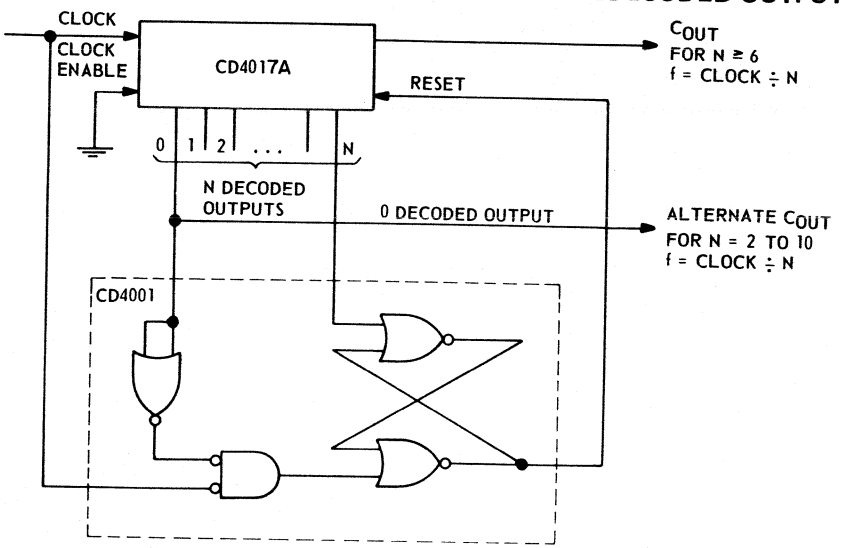
SEQUENCE

Q_3	Q_2	Q_1	STATE
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
0	0	0	0

CIRCUIT NO. 14 – DIVIDE-BY-6 RIPPLE COUNTER (cont'd)

This circuit shows that a single flip-flop section of a CD4013A dual "D" type flip-flop can be added in cascade with the CD4013A divide-by-4 ripple counter shown in Circuit No. 12 to obtain a divide-by-6 ripple counter.

CIRCUIT NO. 15 – DIVIDE-BY-N COUNTER WITH N DECODED OUTPUTS

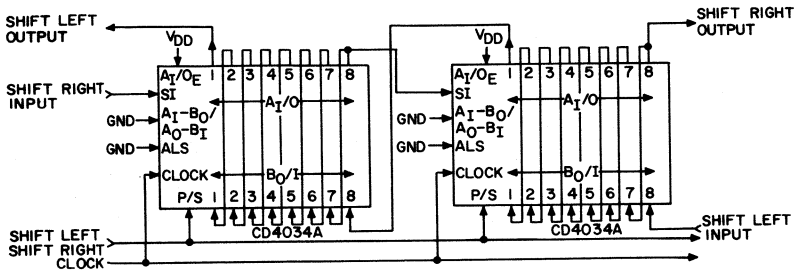


This circuit illustrates the use of a CD4017A decade counter/divider and a CD4001A dual 2-input NOR gate in a divide-by-N counter that provides N decoded outputs. When the Nth decoded output is reached (Nth clock pulse), the S-R flip-flop (constructed from two NOR gates of the CD4001) generates a reset pulse which clears the CD4017A to its zero count. If the Nth decoded output is greater than or equal to 6, the clock-output (C_{OUT}) line goes high to clock the next CD4017A counter section. The "0" decoded output also goes high at this time. Coincidence of a low clock and a low decoded "0" output resets the S-R flip-flop to enable the CD4017A. If the Nth decoded output is less than 6, the C_{OUT} line will not go high and, therefore, cannot be used to clock the next counter. In this case, the "0" decoded output may be used to perform this clocking function.

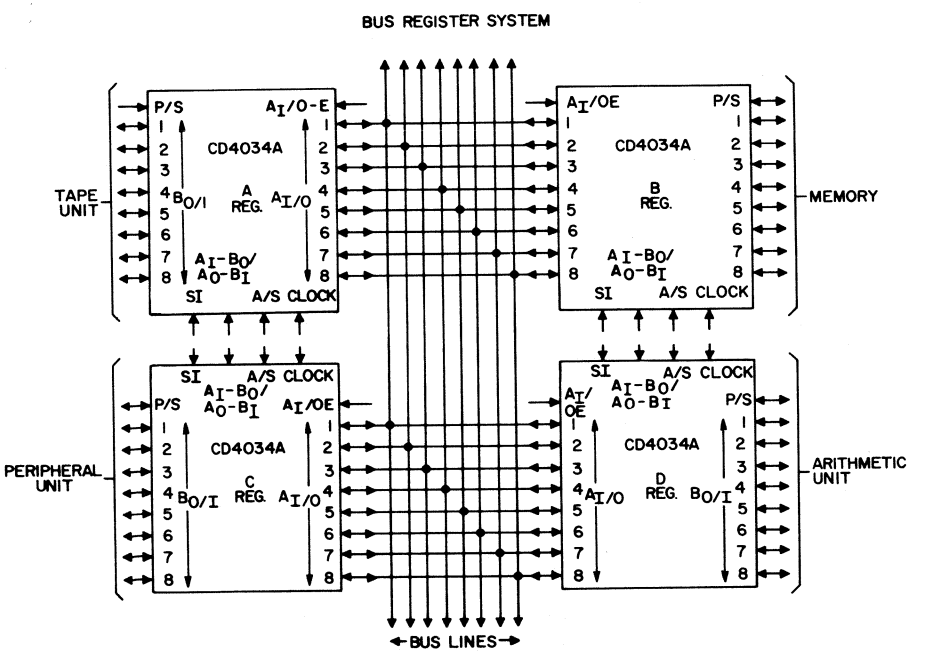
CIRCUIT NO. 16 – SHIFT-LEFT/SHIFT-RIGHT REGISTER

Shift-left/shift-right operations can be performed when two CD4034A shift registers are interconnected as shown in this circuit. For shift-left operation, the P/S control is high; for shift-right operation, and P/S control is low.

CIRCUIT NO. 16 – SHIFT-LEFT/SHIFT-RIGHT REGISTER (cont'd)

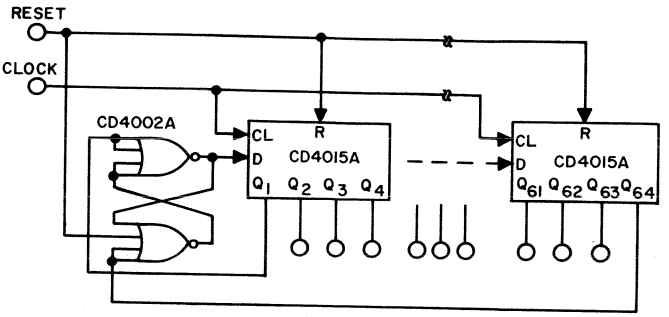


CIRCUIT NO. 17 – BUS REGISTER SYSTEM



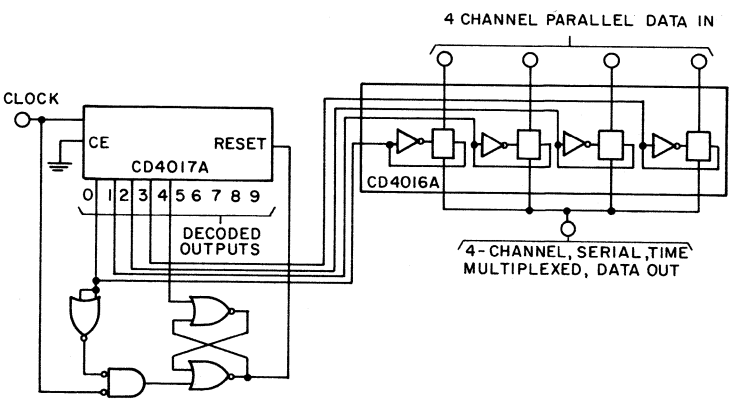
In this circuit, four CD4034A Parallel-In/Parallel-Out shift registers are interconnected to form a bus register system that can effect various register transfers. For example, A Register-to-D Register or D Register-to-A Register, or A Register-to-Bus or Bus-to-C register transfers can be readily achieved. Specific transfers are realized through proper "parallel enable" and "A_I-B_O/A_O-B_I" controls.

CIRCUIT NO. 18 – 64-BIT RING COUNTER



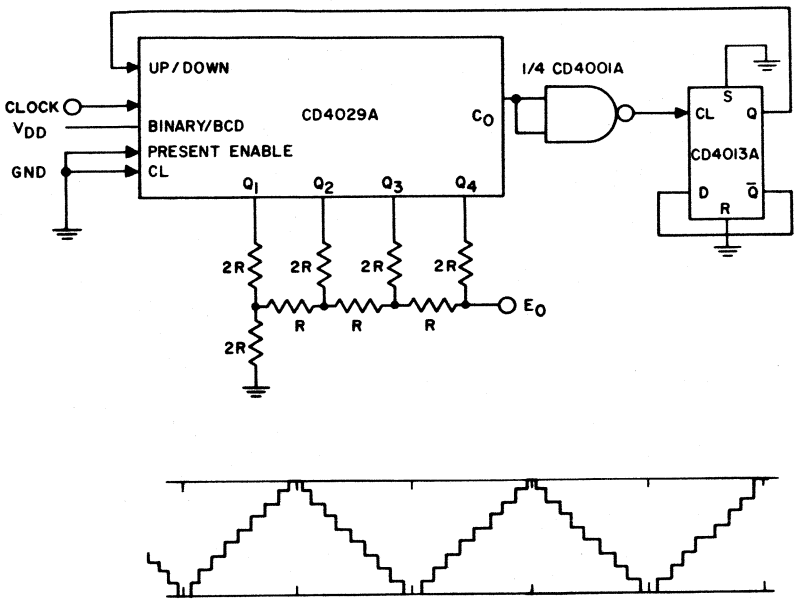
This circuit uses a CD4002A dual four-input NOR gate and eight CD4015A dual 4-stage serial-input/parallel-output shift registers to form a 64-bit ring counter. A reset pulse must be applied for proper starting of the ring counter. The reset pulse causes a "1" to appear at the D input of the first shift register. After the first clock, a "1" appears on Q_1 and resets the control, flip-flop. This "1" now shifts down until it reaches Q_{64} which sets the control flip-flop so that the cycle can repeat. Any desired length other than 64 can be obtained by appropriately varying the number of shift-register stages.

CIRCUIT NO. 19 – FOUR-CHANNEL TIME-DIVISION MULTIPLEXER



This circuit shows a four-channel time-division multiplexer (TDM) that uses a CD4017A decade counter/divider and a CD4016A quad bilateral switch. The CD4017A is operated in a counter-of-4 mode. The decoded outputs of the CD4017A are used to drive each of the four transmission gates of the CD4016A in time sequence.

CIRCUIT NO. 20 – FUNCTION GENERATOR



In this circuit, a CD4029A presettable up/down BCD counter is interconnected with a CD4013A "D"-type flip-flop to generate the "stair-case" waveform shown. As the CD4029A is clocked up to its final count, the clock output C_O goes from a high to a low. This output is inverted by the CD4001A and used to toggle the D flip-flop. This toggling action changes the mode of counting from up to down. When the count gets to 0000, C_O again goes from high to low, and the mode control goes from down to up.

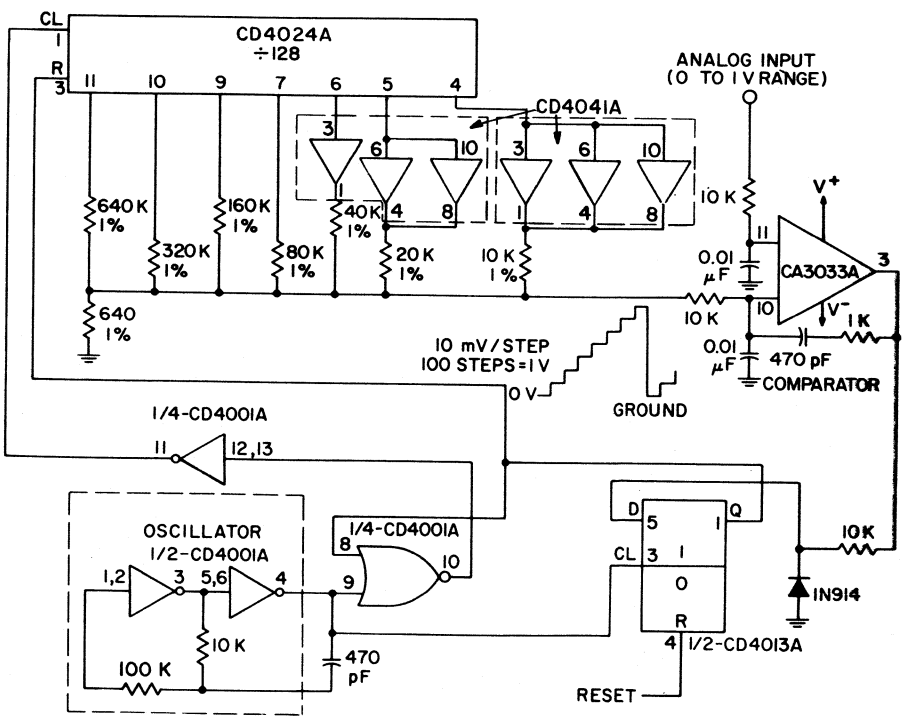
CIRCUIT NO. 21 – DIGITAL RAMP GENERATOR

This digital ramp generator uses several COS/MOS digital integrated circuits (CD4001A, CD4013A, CD4024A, and two CD4041A's) and one bipolar linear integrated circuit (CA3033A). The CD4024A seven-stage ripple counter is operated as a divide-by-28 circuit. This circuit develops a step ramp voltage across a resistor ladder network that includes three sections from each of two CD4041A quad buffers. The number of steps in the ramp is directly related to the count of the CD4024A counter. This ramp voltage is applied to the noninverting input of the

CIRCUIT NO. 21 – DIGITAL RAMP GENERATOR (cont'd)

CA3033A operational amplifier.* The CA3033A compares the amplitude of this voltage with that of the analog voltage applied to its inverting input. When the count of the CD4024A has been reached for which the level of the ramp voltage slightly exceeds that of the analog input, the CA3033A provides an input to the CD4013A "D" type flip-flop, and the Q output of this flip-flop resets the CD4024A counter. The two CD4001A quad four-input NOR-gate-plus-inverter circuits are connected to form an oscillator, NAND gate, and inverter. These circuits provide the clocking for the CD4024A counter and CD4013A flip-flop.

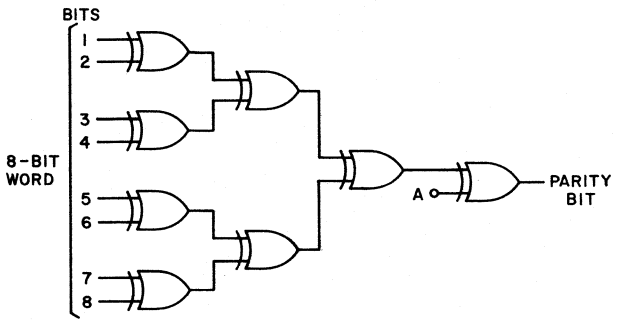
*Detailed descriptive information on the CA3033A is given in the **RCA Linear Integrated Circuits** Manual IC-42 and the RCA Technical Bulletin File No. 360



CIRCUIT NO. 22 – PARITY-BIT GENERATOR

This circuit shows the interconnection of two CD4030A quad exclusive-OR gates to form a parity-bit generator. If the number of "1's" in the 8-bit word is odd, an odd parity bit, i.e., a "1", is generated. Otherwise the output is "0".

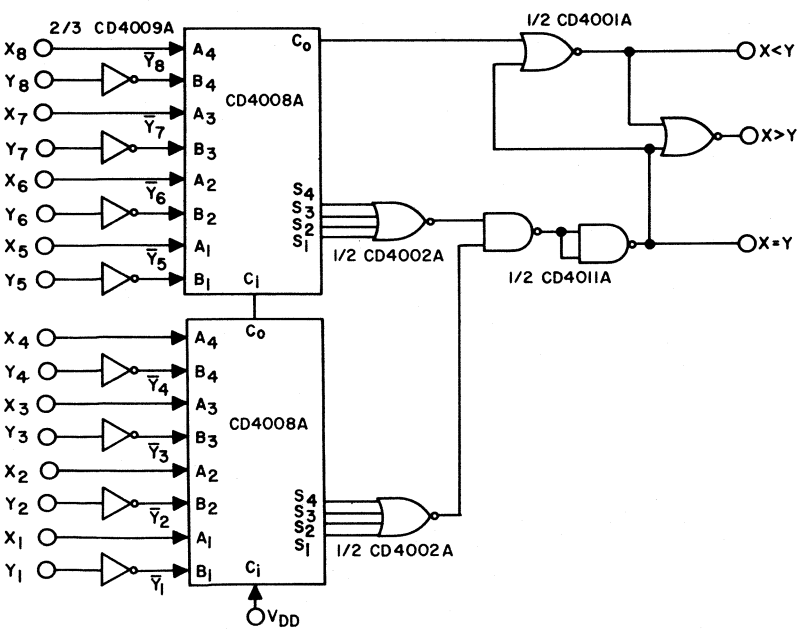
CIRCUIT NO. 22 – PARITY-BIT GENERATOR (cont'd)



A	PARITY
V_{DD}	ODD
GND	EVEN

92CS-17415

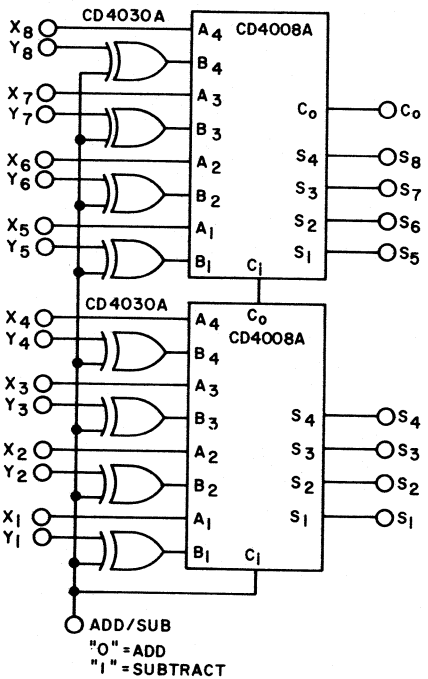
CIRCUIT NO. 23 – EIGHT-BIT MAGNITUDE COMPARATOR



CIRCUIT NO. 23 – EIGHT-BIT MAGNITUDE COMPARATOR (cont'd)

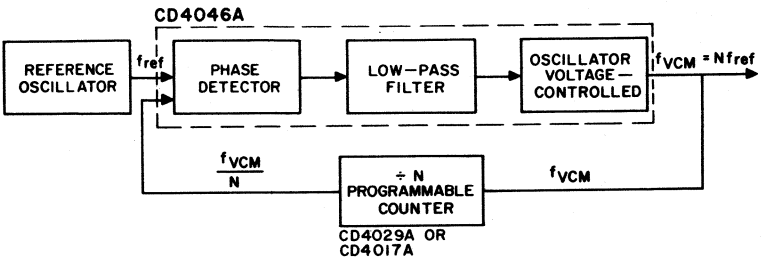
In this circuit, two CD4008A four-bit full adders, one CD4002A dual four-input NOR gate, one CD4001A quad two-input NOR gate, one CD4011A quad two-input NAND gate, and one CD4009A inverting hex buffer are used to compare the magnitudes of two 8-bit numbers. The two's complement of the number $Y_1Y_2 \ldots Y_8$ is added to the second number $X_1X_2 \ldots X_8$. When $X_1X_2 \ldots X_8 = Y_1Y_2 \ldots Y_8$, the X = Y output goes high; when $X_1X_2 \ldots X_8 < Y_1Y_2 \ldots Y_8$, the X < Y output goes high; when $X_1X_2 \ldots X_8 > Y_1Y_2 \ldots Y_8$ the X > Y output goes high.

CIRCUIT NO. 24 – TWO'S-COMPLEMENT ADDER SUBTRACTOR



This circuit illustrates the use of two CD4008A four-bit full adders together with two CD4030A quad exclusive-OR gates to perform two's-complement addition and subtraction. With a "0" on the Add/Sub line, the number $Y_1Y_2 \ldots Y_8$ is not inverted, and the number $X_1X_2 \ldots X_8$ is added to the number $Y_1Y_2 \ldots Y_8$. When "1" is on the Add/Sub line, the number $Y_1Y_2 \ldots Y_8$ is inverted, and the CARRY IN is made a "1" to make the two's complement of the number $Y_1Y_2 \ldots Y_8$. The number $Y_1Y_2 \ldots Y_8$ is added to the number $X_1X_2 \ldots X_8$ to complete the subtraction.

CIRCUIT NO. 25 – PHASE-LOCKED FREQUENCY-SYNTHESIZED LOOP



This block diagram illustrates the use of the CD4046A micropower phase-locked loop in a frequency-synthesizer application. The five basic components of the over-all frequency-synthesized loop include a reference oscillator, a phase detector, a low-pass filter, a voltage controlled multivibrator/oscillator, and a divide-by-N counter. This loop achieves a stable state when $f_{VCO} = Nf_{ref}$. When this condition does not exist, the phase detector forces a change in the VCO frequency until it finds the frequency at which the stable state occurs. The loop locks when the stable state is achieved.

This sytem allows the generation of many discrete frequencies from a single, highly stable source (f_{ref}) and has application in communications (frequency-control systems), computer systems (for synchronizing data tracks and clocking systems), in instruments (frequency synthesizers and counters), and filter networks.

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